ADM5120

HOME GATEWAY CONTROLLER

Datasheet

Version 1.14

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About this Manual

Structure

This Data sheet contains 6 chapters

Chapter 1 Product Overview

Chapter 2 Interface Description

Chapter 3 Function Description

Chapter 4. Register Description

Chapter 5 Electrical Packaging

Chapter 6. Packaging

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Revision History

Date	Version	Change
19 March 2003	1.0	First release of ADM5120
05 June 2003	1.1	3.4, 4.5, 4.6, 4.7, 4.8 and 5.3 sections added. Updated pin numbers.
13 June 2003	1.11	Updated Table for Clock Speeds
08 October 2003	1.12	2.2.5 Memory Bus : A[2] 2.2.10 PCI added CLK I/P 2.2.11 USB added CLK I/P 2.2.14 Corrected pin name 2.2.15 Changed I to O 4.4.1 Switched bits 4.4.11 Removed bits 31 – 17 4.4.12 Bits 31 – 30 bit error 4.4.13 Added bit [6]
29 October	1.13	2.2.5 Added default value to A[0], A[1] & A[13] 2.2.9 Added note
22 December	1.14	1.1 Updated Diagram – removed ADM5106 1.2 Updated features taking out ADM5106 and ECOS refs

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Chapter 1 Product Overview

1.1 Overview

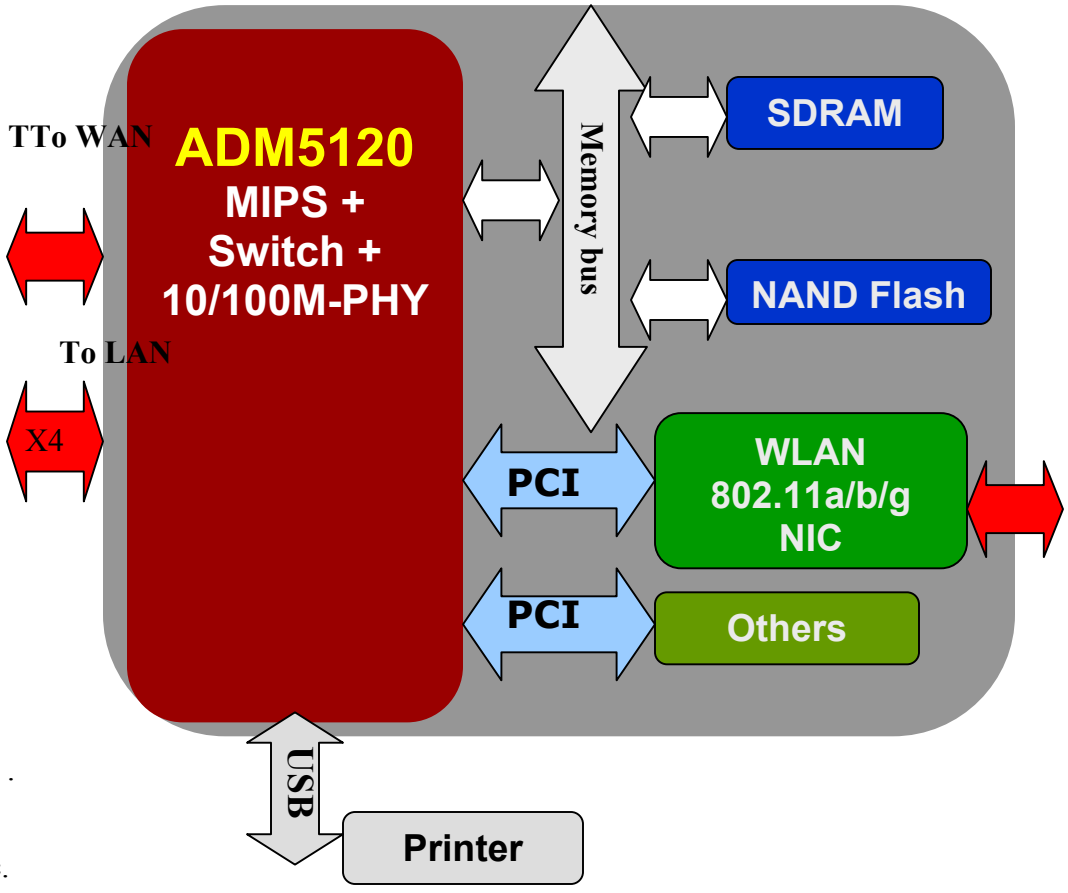
ADM5120 is a high performance, highly integrated, and highly flexible SOC (System-On-Chip) that facilitates the functionalities of SOHO/SME Gateway, NAT Router, Print Server, WLAN Access Point and VPN Gateway. ADM5120 enables the sharing of IP-based broadband services throughout the home/office using wired/wireless computers, entertainment equipment, printers, and other intelligent devices.

Internally, the ADM5120 ASIC consists of a high performance (227 MIPS) embedded MIPS CPU, an embedded switch engine, 10/100M PHY, an embedded PCI bridge, an embedded USB host, and interfaces for UART, SDRAM and Flash. The following diagram illustrates a system configuration that uses the supported functionalities/facilities of ADM5120.

1.1.1 Product Order Information

The ADM5120 comes in two packaging formats as follows:

Section 6.1 Ball Grid Array (BGA) 324-pin
Section 6.2 Plastic Quad Flat Pack (PQFP) 208-pin



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1.2 Features

ASIC Features

Processor

- MIPS 4Kc CPU
- Embedded cache, 8K-byte I-cache, 8K D-cache
- Embedded memory management unit (MMU) – 32-entry TLB, organized as 16 entry pairs
- 175 MHz/227 MIPS

Network

- 6 ports
  - IEEE 802.3 Fast Ethernet
  - 5 auto-MDIX (auto-crossover) twisted paired LAN interfaces, embedded 10/100M PHY
  - 1 GMII(*)/MII interface
  - Flexible WAN port selection
- Embedded switch engine
  - Embedded Data-buffer/Address-look-up table
  - Look-up table read/write-able
  - MAC layer security
  - MAC clone solution
  - Multicast grouping (IGMP)
  - MAC filtering, Bandwidth control
- Class of Services (CoS) with two priority levels
- Shared dynamic data buffer management, embedded SSRAM
- Port grouping VLAN (overlap-able)
- TCP/IP accelerator

Memory interface

- SDRAM
  - Two bank support (2 chip select pins)
  - Each bank can support -- 1Mx32 up to 32Mx32bit (128M-byte)
- Flash
  - NAND Flash boot (*)
  - NOR Flash boot: Two bank support (2 chip select pins)
  - NOR Flash boot: Each bank can support – 1Mx8-bit, up to 1Mx32-bit (4M-byte)

System

- UART interface (support MODEM interface)
- PCI bridge that supports 3 master devices (*)
- GPIO (**)
- USB 1.1 host
- Clock source
  - 25MHz crystal for 10/100
  - 48MHz crystal for USB
- 0.18u CMOS process
- 1.8V/3.3V dual power
- BGA/PQFP

*** Available in BGA only, not PQFP**
**** PQFP has 4 GPIO pins v.s. BGA has 8 pins.**

Software Features

- Linux/Nucleus Real-Time OS
- Linux-based and Nucleus-based turn key support
- Telnet
- IEEE 802.3 Ethernet Driver
- IEEE 802.11 WLAN Driver
- RS232 Driver for Console User Interface
- DHCP Server/Client
- PPP over Ethernet (PPPoE)
- Network Address Translation (NAT) for IP Address Mapping/Sharing/Security
- DNS Proxy
- Simple Network Time Protocol (SNTP)
- Firewall
- Web-Based Configuration: WEB and HTTP
- TFTP upload/download
- IEEE 802.3 SOHO/SME Gateway
- NAT Router
- Single band 802.11g Access Point (through PCI bus: 5120+802.11g NIC)
- Multiple band 802.11a/b/g Access Point (through PCI bus: 5120+802.11a/b/g NIC)
- Print Server (through USB1.1)
- 12-port SME Gateway (through GMII: 5120+6999U)

Typical Applications

1.3 Block Diagram

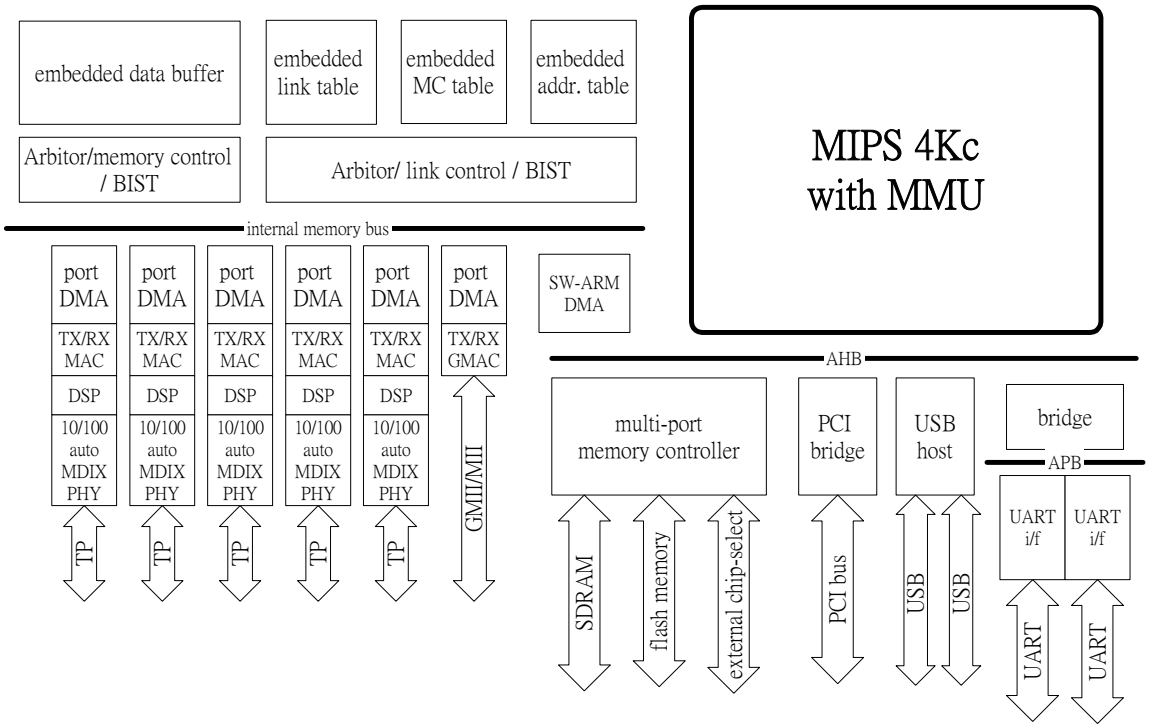

Figure 1-1 ADM5120 Block Diagram

1.4 Abbreviations

AHB	Advance High performance Bus
ALE	Address Latch Enable
AN	Auto-Negotiation
APB	Advanced Peripheral Bus
ASB	Advanced System Bus
ASIC	Application Specific Integrated Circuit
BC	BroadCast
BP	Back Pressure
BPDU	Bridge Protocol Data Unit
BISS	Build In Self test error Skip
BIST	Build In Self Test
CLK	Clock
COL	Collision
CoS	Class of Service
CRC	Cyclic Redundancy Check
CRS	Carrier Sense
CSX	Chip Select for external I/O bank0
DFE	Decision Feedback Equalization
DMA	Direct Memory Access

FC	Flow Control
FIFO	First-In-First-Out
GND	Ground
GPIO	General Purpose I/O
GPIOL	GPIO of groupL
GPIOM	GPIO of groupM
GPSI	General Purpose Serial Interface
HOL	Head-on-Line
INTC	Interrupt Control Registers
INTX	Interrupt for external I/O bank0
IPG	Inter Packet Gap
IRQ	Interrupt ReQuest
JTAG	Joint Test Action Group
LSb	Least Significant Bit
LSB	Least Significant Byte
MAC	Media Access Control
MC	Multicast
MDC	Management Data Clock
MDIO	Management Data I/O
MDI	Medium dependent interface
MDIX	MDI Crossover
MII	Media Independent Interface
MIPS	Million Instructions Per Second
MMU	Memory Management Unit
NAT	Network Address Translation
NRZI	Non Return Zero Invert
NRZ	Non Return Zero
PCS	Physical Coding Sublayer
PHY	PHYsical Layer
PLL	Phase Locked Loop
PMA	Physical Medium Attachment
PMD	Physical medium Dependent
PQFP	Plastic Quad Flat Package
RISC	Reduced Instruction Set Computer
RX	Receive
RXD	Receive Data
RXDV	Receive Data Valid
SA	Source Address
SMC	Flash Control Registers
SW	Switch
SYSC	System Control Registers
TOS	Type Of Service
TX	Transmit
TXC	Transmit Clock
TXE	Transmit Enable
TXD	Transmit Data

UART	Universal Asynchronous Receiver Transmitter
VLAN	Virtual LAN
WAN	Wide Area Networks

1.5 Conventions

1.5.1 Data Lengths

qword	64-bits
dword	32-bits
word	16-bits
byte	8 bits
nibble	4 bits

1.5.2 Register Descriptions

Register Type	***Description***
RO	Read-only
WO	Write-only
RW	Read/Write

1.5.3 Pin Descriptions

Pin Type	***Description***
I	Input
O	Output
BI	BI Directional

Chapter 2 Interface Description

2.1 Pin Assignment

2.1.1 324BGA Ball assignment

	Pin name	Ball		Pin name	Ball		Pin name	Ball		Pin name	Ball
1.	VCCRG	E4	1.	PCI_CBE[1]	U5	1.	DATA[12]	U16	1.	LED2[0]	E14
2.	VCCRG	E4	2.	PCI_CBE[2]	V4	2.	DATA[13]	V17	2.	LED2[1]	A16
3.	VCCBIAS	D3	3.	PCI_CBE[3]	U6	3.	DATA[14]	T17	3.	LED1[2]	B16
4.	VCCBIAS	D3	4.	PCI_AD[31]	W4	4.	DATA[15]	W18	4.	LED1[1]	A15
5.	RTX	C2	5.	DATA[24]	V5	5.	ADDR[13]	V18	5.	LED1[0]	B15
6.	VREF	G5	6.	DQM[0]	T7	6.	ADDR[14]	U17	6.	LED0[2]	A14
7.	CONTROL	F4	7.	DQM[1]	Y4	7.	ADDR[15]	N16	7.	LED0[1]	E13
8.	VCCPLL	D2	8.	SDRAM_CS1_N	W5	8.	PCI_AD[13]	W19	8.	LED0[0]	B14
9.	XO	H5	9.	CAS_N	V6	9.	PCI_AD[12]	V20	9.	CLK48M	A13
10.	XI	G4	10.	RAS_N	T8	10.	PCI_AD[11]	U18	10.	AG33	B13
11.	GCRS	E3	11.	CLK_OUT	Y5	11.	PCI_AD[10]	R18	11.	DG33	B13
12.	GCOL	E2	12.	SDRAM_CS0_N	U8	12.	PCI_AD[9]	V19	12.	DMNS1	C12
13.	G_TXD[7]	F3	13.	ADDR[12]	U7	13.	PCI_AD[8]	N17	13.	DPLS1	B12
14.	G_TXD[6]	E1	14.	ADDR[11]	V7	14.	ADDR[16]	T18	14.	AV33	A12
15.	G_TXD[5]	G3	15.	ADDR[9]	Y6	15.	ADDR[17]	U19	15.	AV33	A12
16.	G_TXD[4]	F2	16.	ADDR[8]	W7	16.	ADDR[18]	U20	16.	DPLS0	B11
17.	G_TXD[3]	F1	17.	PCI_AD[30]	Y7	17.	ADDR[19]	P17	17.	DMNS0	C11
18.	G_TXD[2]	G2	18.	PCI_AD[29]	V8	18.	WE_N	T19	18.	VCCAD	D11
19.	G_TXD[1]	J5	19.	PCI_AD[28]	T9	19.	F_OE_N	M16	19.	VCCAD	D11
20.	G_TXD[0]	G1	20.	PCI_AD[27]	W8	20.	F_CS0_N	T20	20.	RXN4	A10
21.	G_TXC	H1	21.	PCI_AD[26]	Y8	21.	UDCD	R19	21.	RXP4	B10
22.	TXC	J4	22.	PCI_AD[25]	V9	22.	UDSR	P18	22.	TXN4	C10
23.	G_TXE	H2	23.	PCI_AD[24]	U9	23.	UCTS	L17	23.	TXP4	B9
24.	G_RXC	J1	24.	ADDR[10]	W9	24.	UDI0	R20	24.	VCCA2	A9
25.	G_RXDV	K4	25.	ADDR[7]	Y9	25.	UDO0	N18	25.	VCCA2	A8
26.	G_RXD[0]	J2	26.	ADDR[6]	V10	26.	UDI1	P19	26.	TXP3	D9
27.	G_RXD[1]	K5	27.	ADDR[5]	W10	27.	UDO1	L16	27.	TXN3	C9
28.	G_RXD[2]	K3	28.	ADDR[4]	V11	28.	PCI_AD[7]	P20	28.	RXP3	B8
29.	G_RXD[3]	L5	29.	ADDR[0]	Y10	29.	PCI_AD[6]	N19	29.	RXN3	C8
30.	G_RXD[4]	K2	30.	ADDR[1]	U11	30.	PCI_AD[5]	N20	30.	VCCAD	B7
31.	G_RXD[5]	K1	31.	ADDR[2]	Y11	31.	PCI_AD[4]	J16	31.	VCCAD	B7
32.	G_RXD[6]	L1	32.	ADDR[3]	Y12	32.	PCI_AD[3]	M18	32.	RXP2	A7
33.	G_RXD[7]	L2	33.	DQM[3]	T11	33.	PCI_AD[2]	M19	33.	RXN2	A6
34.	MDC	L3	34.	DQM[2]	U12	34.	PCI_AD{1}	M20	34.	TXN2	C7
35.	MDIO	L4	35.	DATA[7]	W12	35.	PCI_AD[0]	L18	35.	TXP2	B6
36.	PCI_DEVSEL	M1	36.	PCI_AD[23]	Y13	36.	PCI_INTA0	K16	36.	VCCA2	B5
37.	PCI_FRAME	M5	37.	PCI_AD[22]	T12	37.	PCI_INTA1	L19	37.	VCCA2	A5
38.	PCI_IRDY	M2	38.	PCI_AD[21]	W13	38.	PCI_INTA2	L20	38.	TXP1	D8
39.	CLE	M3	39.	PCI_AD[20]	Y14	39.	PCI_REQ0	J17	39.	TXN1	D7
40.	ALE	N1	40.	PCI_AD[19]	V13	40.	PCI_REQ1	K18	40.	RXP1	B4
41.	F_CS1_N	N2	41.	PCI_AD[18]	T13	41.	PCI_REQ2	K19	41.	RXN1	B3
42.	NAND_OE_N	N3	42.	DATA[6]	W14	42.	PCI_GNT0	K20	42.	VCCAD	C5
43.	NAND_WE_N	N5	43.	DATA[5]	Y15	43.	PCI_GNT1	J20	43.	VCCAD	C5
44.	WP	M4	44.	DATA[4]	U13	44.	PCI_GNT2	J19	44.	RXN0	D6
45.	RDY	P1	45.	DATA[8]	T14	45.	PCI_RESET	H16	45.	RXP0	E7
46.	SP	P2	46.	DATA[9]	W15	46.	PCI_CLK33	J18	46.	TXN0	C4
47.	DATA[16]	P3	47.	DATA[10]	Y16	47.	TRST_N	H20	47.	TXP0	C3
48.	PCI_TRDY	R1	48.	DATA[11]	V15	48.	TDI	H19	48.	VCCA2	D4
49.	PCI_SER	R2	49.	DATA[3]	W16	49.	TDO	G20	49.		
50.	DATA[17]	R3	50.	DATA[2]	Y17	50.	TMS	G19	50.	GNDR/T	E12

	Pin name	Ball		Pin name	Ball		Pin name	Ball		Pin name	Ball
51.	DATA[18]	R4	51.	DATA[1]	V16	51.	TCK	H18	51.	GNDR/T	E11
52.	DATA[19]	T1	52.	DATA[0]	W17	52.	LED4[2]	F20	52.	GNDR/T	D10
53.	DATA[31]	P5	53.	PCI_AD[17]	U15	53.	LED4[1]	G18	53.	GNDR/T	E10
54.	PCI_PAR	T2	54.	PCI_AD[16]	Y18	54.	LED4[0]	F19	54.	GNDR/T	E9
55.	PCI_PERR	T3	55.	PCI_AD[15]	Y19	55.	LED3[2]	G16	55.		
56.	PCI_STOP	U2	56.	PCI_AD[14]	Y20	56.	LED3[1]	E20	56.	VDD	F17
57.	DATA[30]	U1	57.			57.	LED3[0]	D20	57.	VDD	D13
58.	DATA[29]	W1	58.	VSS	N12	58.	LED2[2]	E19	58.	VDD	D12
59.	DATA[28]	V2	59.	VSS	N11	59.	GPIO[0]	F18	59.	VDD	V14
60.	DATA[20]	Y1	60.	VSS	L10	60.	GPIO[1]	D19	60.	VDD	V12
61.	DATA[21]	W2	61.	VSS	M10	61.	GPIO[2]	G17	61.	VDD	U10
62.	DATA[22]	U3	62.	VSS	N10	62.	GPIO[3]	E18	62.	VDD	T10
63.	DATA[23]	T4	63.	VSS	V1	63.	GPIO[4]	C20	63.	VDD	H3
64.	DATA[27]	V3	64.	VSS	Y3	64.	GPIO[5]	C19	64.	VDD	H4
65.	DATA[26]	Y2	65.	VSS	N8	65.	GPIO[6]	D18	65.	VDD	K17
66.	DATA[25]	W3	66.	VSS	N9	66.	GPIO[7]	E17	66.	VDD	P16
67.	PCI_CBE[0]	U4	67.	VSS	M8	67.	TEST	C18	67.		
68.			68.	VSS	K8	68.	RESET_N	B18	68.	DVDD	J3
69.	GNDRG	C1	69.	VSS	H9	69.	CLKO25M	D17	69.	DVDD	D14
70.	GNDRG	B1	70.	VSS	J9	70.	CLKO33M	C17	70.	DVDD	D15
71.	VSS	H11	71.	VSS	H10	71.			71.	DVDD	H17
72.	VSS	H12	72.	VSS	J10	72.	VSS	L8	72.	DVDD	W6
73.	VSS	A11	73.	VSS	K10	73.	VSS	M9	73.	DVDD	W11
74.	VSS	A20	74.	VSS	K9	74.	VSS	M11	74.	DVDD	U14
75.	VSS	A19	75.	VSS	B2	75.	VSS	M12	75.	DVDD	R17
76.	VSS	A18	76.	VSS	A1	76.	VSS	W20	76.	DVDD	M17
77.	VSS	A17	77.	VSS	A2	77.	VSS	N13	77.	DVDD	N4
78.	VSS	B17	78.	VSS	A3	78.	VSS	M13	78.	DVDD	P4
79.	VSS	D16	79.	VSS	A4	79.	VSS	L11	79.		
80.	VSS	C16	80.	VSS	C6	80.	VSS	L12	80.	VSS	J13
81.	VSS	C15	81.	VSS	D5	81.	VSS	K13	81.	VSS	K11
82.	VSS	C14	82.	VSS	E8	82.	VSS	J11	82.	VSS	K12
83.	VSS	C13	83.	VSS	H8	83.	VSS	J12	83.	VSS	L13
84.	VSS	H13	84.	VSS	J8	84.			84.		

Table 2-1 ADM5120 324 BGA Pin Assignment

2.1.2 208PQFP pin assignment

	Pin name		Pin name		Pin name		Pin name
1.	VCCRG	53.	VSS	105.	DATA[12]	157.	DVSS
2.	VCCBIAS	54.	DATA[24]	106.	DATA[13]	158.	LED2[0]
3.	RTX	55.	DQM[0]	107.	DATA[14]	159.	DVDD
4.	GNDRG	56.	DQM[1]	108.	DATA[15]	160.	LED2[0]
5.	VREF	57.	VDD	109.	ADDR[13]	161.	LED1[2]
6.	CONTROL	58.	SDRAM_CS1_N	110.	ADDR[14]	162.	LED1[1]
7.	GNDPLL	59.	CAS_N	111.	VSS	163.	LED1[0]
8.	VCCPLL	60.	RAS_N	112.	DVSS	164.	LED0[2]
9.	XO	61.	DVSS	113.	ADDR[15]	165.	LED0[1]
10.	XI	62.	CLK_OUT	114.	VDD	166.	LED0[0]
11.	DVSS	63.	DVDD	115.	DVDD	167.	VSS
12.	GCRS	64.	SDRAM_CS0_N	116.	ADDR[16]	168.	CLK48M
13.	GCOL	65.	ADDR[12]	117.	ADDR[17]	169.	VDD
14.	G_TXD[3]	66.	ADDR[11]	118.	ADDR[18]	170.	AG33
15.	G_TXD[2]	67.	ADDR[9]	119.	ADDR[19]	171.	DMNS1
16.	G_TXD[1]	68.	ADDR[8]	120.	WE_N	172.	DPLS1
17.	G_TXD[0]	69.	VSS	121.	F_OE_N	173.	AV33
18.	VDD	70.	VDD	122.	F_CS0_N	174.	DPLS0
19.	TXC	71.	ADDR[10]	123.	UDCD	175.	DMNS0
20.	G_TXE	72.	ADDR[7]	124.	UDSR	176.	VCCAD
21.	VSS	73.	ADDR[6]	125.	UCTS	177.	RXN4
22.	G_RXC	74.	ADDR[5]	126.	DVSS	178.	RXP4
23.	DVDD	75.	ADDR[4]	127.	UDI0	179.	GNDT
24.	G_RXDV	76.	ADDR[0]	128.	DVDD	180.	TXN4
25.	G_RXD[0]	77.	DVSS	129.	UDO0	181.	TXP4
26.	G_RXD[1]	78.	VSS	130.	UDI1	182.	VCCA2
27.	G_RXD[2]	79.	ADDR[1]	131.	UDO1	183.	VCCA2
28.	G_RXD[3]	80.	DVDD	132.	VSS	184.	TXP3
29.	MDC	81.	ADDR[2]	133.	VDD	185.	TXN3
30.	MDIO	82.	ADDR[3]	134.	TRST_N	186.	GNDR
31.	RDY	83.	DQM[3]	135.	TDI	187.	RXP3
32.	DVSS	84.	DQM[2]	136.	TDO	188.	RXN3
33.	DATA[16]	85.	DATA[7]	137.	TMS	189.	VCCAD
34.	DVDD	86.	VDD	138.	DVSS	190.	RXP2
35.	DATA[17]	87.	VSS	139.	TCK	191.	RXN2
36.	DATA[18]	88.	DATA[6]	140.	DVDD	192.	GNDR
37.	DATA[19]	89.	DATA[5]	141.	LED4[2]	193.	TXN2
38.	DATA[31]	90.	DATA[4]	142.	LED4[1]	194.	TXP2
39.	VSS	91.	DATA[8]	143.	LED4[0]	195.	VCCA2
40.	DATA[30]	92.	DATA[9]	144.	LED3[2]	196.	VCCA2
41.	VDD	93.	DVSS	145.	LED3[1]	197.	TXP1
42.	DATA[29]	94.	DVSS	146.	LED3[0]	198.	TXN1
43.	DATA[28]	95.	DATA[10]	147.	LED2[2]	199.	GNDR
44.	DATA[20]	96.	DVDD	148.	GPIO[0]	200.	RXP1
45.	DVSS	97.	VDD	149.	GPIO[1]	201.	RXN1
46.	DATA[21]	98.	DATA[11]	150.	GPIO[2]	202.	VCCAD
47.	DVDD	99.	DATA[3]	151.	GPIO[3]	203.	RXN0
48.	DATA[22]	100.	DATA[2]	152.	TEST	204.	RXP0
49.	DATA[23]	101.	DATA[1]	153.	RESET_N	205.	GNDT
50.	DATA[27]	102.	DATA[0]	154.	VDD	206.	TXN0
51.	DATA[26]	103.	VSS	155.	CLKO25M	207.	TXP0
52.	DATA[25]	104.	VSS	156.	VSS	208.	VCCA2

Table 2-2 ADM5120 208PQFP Pin Assignments

2.2 Pin Description by Function

ADM5120 pins are categorized into one of the following groups:

- Section 2.2.1 Network Media Connection
- Section 2.2.2 Clock for Network
- Section 2.2.3 LED
- Section 2.2.4 GMII/MII Management
- Section 2.2.5 Memory Bus
- Section 2.2.6 SDRAM Control Signals
- Section 2.2.7 UART
- Section 2.2.8 JTAG
- Section 2.2.9 General Purpose I/O (GPIO)
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Section

- 2.2.14 Power and Ground
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- Section 2.2.16 Miscellaneous

Note: All default settings are 0.

2.2.1 Network Media Connection

Pin Name	BGA Ball	PQFP Pin#	Type	Descriptions
RXP[4:0]	B10, B8, A7, B4, E7	178, 187, 190, 200, 204	I	Receive Pair. Differential data is received on these pins.
RXN[4:0]	A10, C8, A6, B3, D6	177, 188, 191, 201, 203	I	
TXP[4:0]	B9, D9, B6, D8, C3	181, 184, 194, 197, 207	O	Transmit Pair. Differential data is transmitted on these pins.
TXN[4:0]	C10, C9, C7, D7, C4	180, 185, 193, 198, 206	O	

2.2.2 Clock for Network

Pin Name	BGA Ball	PQFP Pin#	Type	Descriptions
XOI	H5	9	O	25 MHz crystal
XI	G4	10	I	25 MHz crystal, external clock input
RTX	C2	3	I	Reference Voltage

2.2.3 LED

Pin Name	BGA Ball	PQFP Pin#	Type	Descriptions
LED4[2:0]	F20, G18, F19	141, 142, 143	O	LED4[2] state, default = 1010, duplex/col LED4[1] state, default = 0101, speed LED4[0] state, default = 1001, link/activity
LED3[2:0]	G16, E20, D20	144, 145, 146	O	LED3[2] state, default = 1010, duplex/col LED3[1] state, default = 0101, speed LED3[0] state, default = 1001, link/activity
LED2[2:0]	E19, E14, A16	147, 158, 160	O	LED2[2] state, default = 1010, duplex/col LED2[1] state, default = 0101, speed LED2[0] state, default = 1001, link/activity
LED1[2:0]	B16, A15, B15	161, 162, 163	O	LED1[2] state, default = 1010, duplex/col

Pin Name	BGA Ball	PQFP Pin#	Type	Descriptions
				LED1[1] state, default = 0101, speed LED1[0] state, default = 1001, link/activity
LED0[2:0]	A14, E13, B14	164, 165, 166	O	LED0[2] state, default = 1010, duplex/col LED0[1] state, default = 0101, speed LED0[0] state, default = 1001, link/activity

Note:
Registers, not hardware pins, control the LED display. There are 3 LEDs per port, and they can be programmed to any state, the programming information can be found in Table 2-1 below.
Note: to avoid the SSO problem, shift 10ns between each LED enable.

Function	State
GPIO_in (or GPIO_disable)	0000
GPIO_output_flash	0001
GPIO_output_0	0010
GPIO_output_1	0011
link (steady)	0100
speed (steady)	0101
duplex (steady)	0110
activity (flash)	0111
collision (flash)	1000
link+activity	1001
duplex+collision	1010
10M_link+activity	1011
100M_link+activity	1100
Reserved	1101
Reserved	1110
Reserved	1111

Table 2-3 LED Program Table

2.2.4 GMII/MII Management

Pin Name	BGA Ball	PQFP Pin#	Type	Descriptions
MII Management for MII_0, and MII_1 port. All can be floated if no MII need.				
MDC	L3	29	O	Clock input MDIO. It runs at a 1MHz frequency clock for MII port auto-negotiation result monitoring.
MDIO	L4	30	BI	Internal pull down. Bi-directional serial pin used to write and read form the registers of the device.

Pin Name	BGA Ball	PQFP Pin#	Type	Descriptions
MII_0 Interface, if no need, let all pins be floated				
GCRS	E3	12	I	Carrier Sense, Internal pull down.
GCOL	E2	13	I	Collision, Internal pull down.
G_TXD[7:0]/G_TXD[3:0]	F3, E1, G3, F2, F1, G2, J5, G1	14, 15, 16, 17	O	Transmit Data, all internal pull down. (1)The force speed, duplex & flow control can be set by switch control register (B+14) (2) The reverse MII can only be set by switch control register (B+30)
G_TXE	H2	20	O	Transmit Enable, Internal pull down.
GTXC	H1	NA	O	Transmit Clock, Internal pull down.
TXC	J4	19	I	Transmit Clock, Internal pull down.
GRXC	J1	22	I	Receive Clock, Internal pull down.
GRXDV	K4	24	I	Receive Data Valid, internal pull down
GRXD[7:0]/RXD[3:0]	L2, L1, K1, K2, L5, K3, K5, J2	28, 27, 26, 25	I	Receive Data, internal pull down

2.2.5 Memory Bus

Pin Name	BGA Ball	PQFP Pin#	Type	Descriptions
DATA[31:0]	P5, U1, W1, V2, V3, Y2, W3, V5, T4, U3, W2, Y1, T1, R4, R3, P3, W18, T17, V17, U16, V15, Y16, W15, T14, W12, W14, Y15, U13, W16, Y17, V16, W17	38, 40, 42, 43, 50, 51, 52, 54, 49, 48, 46, 44, 37, 36, 35, 33, 108, 107, 106, 105, 98, 95, 92, 91, 85, 88, 89, 90, 99, 100, 101, 102	BI	Internal pull down. Data bus for SDRAM, flash memory, and external device
ADDR[19:0]	P17, U20, U19, T18, N16, U17, V18, U7, V7, W9, Y6, W7, Y9, V10, W10, V11, Y12, Y11, U11, Y10	119, 118, 117, 116, 113, 110, 109, 65, 66, 71, 67, 68, 72, 73, 74, 75, 82, 81, 79, 76	O	Address bus for SDRAM, flash memory, and external device. (1) A[19]: Internal pull down. Pull down = Little Endian. (default) (2) A[18:17]: Internal pull down. Can be pulled up and down as following: 00 : boot in 8-bit (Flash memory) (default) 01 : boot in 16-bit 10 : boot in 32-bit. 11: Reserved (3) A[16:14]: Test mode purpose (4) A[13]: Default value: 0 1: PHY separate power on enable 0: PHY separate power on disable (5) A[12]:

Pin Name	BGA Ball	PQFP Pin#	Type	Descriptions
				0: BGA package 1: 208 PQFP package (6) A[4:3]: Can be pulled up and down as following: PLL frequency setting 00: 175MHz (Default) 01: 200MHz 1x: Reserved (7)A[2]: 0: Enable AutoMDIX 1: Disable AutoMDIX (Default) (8) A[1]: Default value: 0 1: NAND boot enable 0: NAND boot disable (9) A[0]: Default value: 0 1: Simulation mode 0: Normal operation

2.2.6 SDRAM Control Signals

Pin Name	BGA Ball	PQFP Pin#	Type	Descriptions
CLK_OUT	Y5	62	O	SDRAM clock, the frequency is set by A[4:3] 00: 87.5MHz (Default) 01: 100MHz ***Note:*** 1=pull up, 0=pull down
SDRAM_CS0_N	U8	64	O	SDRAM chip select 1
RAS_N	T8	60	O	Raw address strobe, active low
CAS_N	V6	59	O	Column address strobe, active low
SDRAM_CS1_N	W5	58	O	SDRAM chip select 1
DQM[3:0]	T11, U12, T7, Y4	83, 84, 55, 56	O	Data mask output to SDRAM
F_CS0_N	T20	122	O	Chip select for external memory, like flash, bank0, active low
F_CS1_N	N2	NA	O	Chip select for external memory, like flash, bank1, active low
F_OE_N	M16	121	O	Output enable for external memory banks, active low
WE_N	T19	120	O	Write Enable for external memory banks and SDRAM

2.2.7 UART

Pin Name	BGA Ball	PQFP Pin#	Type	Descriptions
UDCD	R19	123	I	UART0 Data carrier detect (modem status input), active low Can also be used as GPIO
UDSR	P18	124	I	UART0 Data set ready (modem status input), active low Can also be used as GPIO

UCTS	L17	125	I	UART0 clear to send (modem status input), active low Can also be used as GPIO
UDI0	R20	127	I	UART0 receive serial data input, Internal pull down.
UDO0	N18	129	O	UART0 transmit serial data output
UDI1	P19	130	I	UART1 receive serial data input, Internal pull down.
UDO1	L16	131	O	UART1 transmit serial data output

2.2.8 JTAG

Pin Name	BGA Ball	PQFP Pin#	Type	Descriptions
TCK	H18	139	I	JTAG test clock, Internal pull down.
TMS	G19	137	I	JTAG test mode select, Internal pull down.
TDO	G20	136	O	JTAG test data out
TDI	H19	135	I	JTAG test data in, Internal pull down.
TRST_N	H20	134	I	JTAG asynchronous reset (active low)

2.2.9 General Purpose I/O (GPIO)

Pin Name	BGA Ball	PQFP Pin#	Type	Descriptions
GPIO[7:0]/GPIO[3:0]	E17, D18, C19, C20, E18, G17, D19, F18	151, 150, 149, 148	BI	BI General purpose I/O pin. GPIO[0] is internal pull up. GPIO[2:1] are internal pull down. Note: In the BGA version GPIO5 can be programmed to SDRAM memory address A20 for 2Mx16bit Flash thus supporting large Flash memory.
LEDN[2:0]	Refer to LED section	Refer to LED section	BI	General purpose I/O pin GPIO[8:3] are internal pull down.

2.2.10 PCI

Pin Name	BGA Ball	PQFP Pin#	Type	Descriptions
PCI_AD[31:0]	W4, Y7, V8, T9, W8, Y8, V9, U9, Y13, T12, W13, Y14, V13, T13, U15, Y18, Y19, Y20, W19, V20, U18, R18, V19, N17, P20, N19, N20, J16, M18, M19, M20, L18	NA	BI	Address and data bus are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phase. The PCI host bridge support both read and write bursts.
PCI_CBE[3:0]	U6, V4, U5, U4	NA	BI	Bus Command and Byte Enables
PCI_DEVSEL	M1	NA	BI	Device Select. When actively indicates the driving device has decoded its address as the target of the current access.
PCI_FRAME	M5	NA	BI	Cycle Frame. PCI_FRAME is asserted to indicate a bus transaction is beginning and data transfers continue

Pin Name	BGA Ball	PQFP Pin#	Type	Descriptions
PCI_GNT[2:0]	J19,J20,K20	NA	O	Grant. It indicates to the master that access to the PCI bus has been granted
PCI_IRDY	M2	NA	BI	Initiator Ready.
PCI_PAR	T2	NA	BI	Parity
PCI_PERR	T3	NA	BI	Parity Error
PCI_REQ[2:0]	K19,K18,J17	NA	I	PCI Bus Request
PCI_SER	R2	NA	BI	System Error
PCI_STOP	U2	NA	BI	Stop indicates the current target is requesting the host to stop the current transaction due to unusual condition
PCI_TRDY	R1	NA	BI	Target Ready.
PCI_INTA[2:0]	L20,L19,K16	NA	I	PCI interrupt input
PCI_RESET	H16	NA	O	PCI bus Reset.
PCI_CLK33	J18	NA	I	PCI bus Clock input.
PCI_CLK33	C17	NA	0	PCI bus Clock output.

2.2.11 USB

Pin Name	BGA Ball	PQFP Pin#	Type	Descriptions
DMNS1	C12	171	BI	Data- of USB port1. differential data bus conforming to the USB 1.1
DPLS1	B12	172	BI	Data+ of USB port1. differential data bus conforming to the USB 1.1
DMNS0	C11	175	BI	Data- of USB port0. differential data bus conforming to the USB 1.1
DPLS0	B11	174	BI	Data+ of USB port0. differential data bus conforming to the USB 1.1
CLK48M	A13	168	I	USB Clock Input

2.2.12 NAND Flash

Pin Name	BGA Ball	PQFP Pin#	Type	Descriptions
NAND_OE_N	N3	NA	O	Read enable
NAND_WE_N	N5	NA	O	Write enable
CLE	M3	NA	O	Command Latch Enable
ALE	N1	NA	O	Address Latch Enable
WP	M4	NA	O	Write Protect
RDY	P1	NA	I	Ready/Busy Input
SP	P2	NA	O	Spare enable

2.2.13 External CS/INT/wait

Pin Name	BGA Ball	PQFP Pin#	Type	Descriptions
WAIT#	F18	148	I	WAIT# is available in en_csx_intx and en_wait enable. See switch control register GPIO_config2 (B+BC), bit[4], bit[5], and bit[6]. When CSX active and SMC programmable wait_state time-out, then check the WAIT# if high, then complete the access

Pin Name	BGA Ball	PQFP Pin#	Type	Descriptions
				if low, then wait until WAIT# go high
CSX0#	D19	149	O	External chip select, active low, available if en_csx_intx enable in the switch control register GPIO_config2 (B+BC), bit[4]
INTX0	G17	150	I	External interrupt input, active high, available if en_csx_intx enable in the switch control register GPIO_config2 (B+BC), bit[4]
CSX_1#	E18	151	O	External chip select 1, active low, available if en_csx_intx_1 enable in the switch control register GPIO_config2 (B+BC), bit[5]
INTX1#	C20	NA	I	Internal pull down. external interrupt input 1, active high, available if en_csx_intx_1 enable in the switch control register GPIO_config2 (B+BC), bit[5]

2.2.14 Power and Ground

Pin Name	BGA Ball	PQFP Pin#	Type	Descriptions
VDD	F17, D13, D12, V14, V12, U10, T10, H3, H4, K17, P16	18, 41, 57, 70, 86, 97, 114, 133, 154, 169		Positive Power for Digital Core,1.8V
DVDD	J3, D14, D15, H17, W6, W11, U14, R17, M17, N4, P4	23, 34, 47, 63, 80, 96, 115, 128, 140, 159		Positive Power for I/O, 3.3V
VDDA2	D4, A5, B5, A8, A9	182, 183, 195, 196, 208		Positive Power for Analog circuitry, 1.8V
VCCAD	C5, B7, D11	176, 189, 202		Positive Power for Analog circuitry, 3.3V
VSS	H11, H12, A11, A20, A19, A18, A17, B17, D16, C16, C15, C14, C13, H13, N12, N11, L10, M10, N10, V1, Y3, N8, N9, M8, K8, H9, J9, H10, J10, K10, K9, B2, A1, A2, A3, A4, C6, D5, E8, H8, J8, L8, M9, M11, M12, W20, N13, M13, L11, L12, K13, J11, J12, J13, K11, K12, L13	7, 11, 21, 32, 39, 45, 53, 61, 69, 78, 77, 87, 93, 94, 103, 104, 111, 112, 126, 132, 138, 156, 157, 167		GND for Digital circuit
VSSA	E12, E11, D10, E10, E9	205, 199, 192, 186, 179		GND for Analog circuitry
VCCPLL	D2	8		Power for Phase Lock Loop, 1.8V
VCCRG	E4	1		Power for Regulator, 3.3V
VCCBIAS	D3	2		Power for BIAS, 3.3V
GNDRG	C1, B1	4		Ground
AV33	A12	173		Power for USB PHY, 3.3V
AG33	B13	170		Power for USB GND

2.2.15 Regulator Interface

Pin Name	BGA Ball	PQFP Pin#	Type	Descriptions
VREF	G5	5	I	Reference Voltage Input
CONTROL	F4	6	0	FET Control Output (for 3.3V to 1.8V Regulation)

2.2.16 Miscellaneous

Pin Name	BGA Ball	PQFP Pin#	Type	Descriptions
TEST	C18	152	I	TEST pin
RESET_N	B18	153	I	System reset, active low

Chapter 3 Function Description

3.1 System

3.1.1 Frequency

The system clock frequency of ADM5120 is programmable as follows

00: 175MHz (Default)
01: 200MHz
1x: Reserved

The number is set by the pull up or pull down of A[4:3].
This clock is for the MIPS, major switch cores, and SDRAM access.

3.1.2 Boot code data-width

The data width of flash or ROM is set by A[19:17] pull up or down
A[19:17] → 1xx: Big-Endian (default 0: little endian)

x00: boot in 8-bit (default)
x01: boot in 16-bit
x10: boot in 32-bit
11: Reserved

3.1.3 GMII/MII port

The GMII/MII port can be programmed for the following: AN monitor on/off, force speed/duplex/flow-control, which can be set by Switch Control Register (B+14).

The GMII/MII direction is also programmable for the following: connect to PHY or AC, which can be set by Switch Control Register (B+30).

The default GMII/MII mode is 'connect to PHY'. The signals direction will change, and suggest the connection as below

(5120 PHY)	RXC	→	RXC (MAC side)
	TXC	→	TXC
	TXD	→	RXD
	TXE	→	RXDV
	RXD	←	TXD
	RXDV	←	TXE
	COL	→	COL
	CRS	→	CRS

3.2 PHY

3.2.1 PHY Overview

The ADM5120 is an embedded 5 ports Ethernet PHY device. It is capable of operating at either 10Mbps or 100Mbps. The PHY is associated with the Physical Layer of the OSI model. The PHY performs functions between the Medium Dependent Interface (MDI) and the internal MAC of switch. According to the IEEE 802.3u, the PHY contains the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), Physical medium Dependent (PMD), and the optional Auto- Negotiation functions.

In the 100BASE-TX mode, the internal PHY takes the data from the MACs then performs the physical layer 4B/5B encoding, scrambling, parallel to serial conversion, NRZ to NRZI conversion, and NRZI to MLT-3 conversion for transmission over the UTP CAT 5 cable.

The receive paths use an adaptive equalizer to take MLT-3 signals from the cable, performs clock recovery, performs a MLT-3 to NRZI conversion, a NRZI to NRZ conversion, de-scrambling the data, 4B/5B decoding, performs data alignment, stores the data in an elasticity buffer and then converts to nibble data that is applied to the MACs. Auto-Negotiation, carrier sense, collision detection is implemented in the device logic.

Similarly, in the 10BASE-T mode, Manchester encoding and decoding is used with two level transmitted and received data on CAT 3 cable.

3.2.2 Link Detect

The 10Base-T and the 100Base-TX have different means of signaling link integrity. The link detect function uses a counter to count the number of edges in the receive signal over a given period. When enough edges are counted on three consecutive periods, link detect is established. The number of edges will determine whether the link is 10Base-T or 100Base-TX.

3.2.3 Auto-Negotiation

An Auto-Negotiation (AN) mechanism as defined in the IEEE 802.3u is implemented. When AN function is enabled, the mode of operation will be automatically chosen by advertising its abilities and comparing them with those received from its link partner. Each transceiver port can advertise 100Base-Tx full duplex, 100Base-T half duplex, and 10Base-T full or half duplex. Each transceiver will negotiate independently with its link partner and choose the highest level of operation available for its own link. The CPU can set this enable/disable/force via the registers.

3.2.4 Digital Adaptive Equalizer

100Base-TX transmission through the transmission media causes signal distortion characterized as wideband loss, baseline wander, jitter, frequency errors, and intersymbol

interference. The adaptive equalizer function conditions the incoming 100Base-T receive signal to compensate for this distortion. Transceivers that utilize an analog methodology to equalize are subject to system noise degrading their performance while a digital methodology provides better noise immunity but with the tradeoff of high power consumption. This design uses an optimal combination of analog and digital techniques resulting in superior performance in signal recovery and with low power consumption. This equalizer uses forward analog equalization and digital decision feedback equalization (DFE). Gain, offset, baseline wander, jitter and frequency error are addressed and compensated. This technique enables outstanding performance up to 100meters on CAT 5 twisted pair even in noisy environments. 10Base-T transmission, utilizes a pre-equalization technique, the adaptive equalizer is bypassed.

3.2.5 Clock Recovery

The clock recovery function is based on Phase Locked Loop (PLL). The clock samples the equalized signal with a feedback mechanism to shift the sampling point to the optimum position. This recovered clock is used to synchronize all other functions of the "Receive" section especially data recovery and data transmittal.

3.2.6 Stream Cipher Scrambler/ De-scrambler

To reduce the radiated emissions on the twisted pair cable, a scrambling function is implemented to randomize the data. The TX data is combined with an 11bit wide linear shift register producing a 2047 bit non-repeating sequence.
The de-scrambling function requires that the data is synchronized and aligned. The de-scrambler monitors the recovered data for a sequence representing idle codes to achieve synchronization with the transmit shift register. Once the pattern is deciphered, the data can then be retrieved for further processing.

3.2.7 Encoder/Decoder

To reduce the radiated emissions, ensure bandwidth spread, ensure sufficient signal transitions for clock recovery, and provide framing for the 100Base-TX mode, the IEEE 802.3 provides for a 4B(4bit data nibble) to 5B (5 bit symbol) conversion. As well, the MLT-3 line coding was introduced to limit signal transitions and to half peak value per cycle. Thus significantly reducing the FCC emissions above 30 MHz. Thus the signal is encoded for transmission along the line and decoded upon when signal reaches destination.

3.3 Switch Engine

3.3.1 Hashing Function

ADM5120 provides an embedded 1K MAC address look-up table to implement the address recognition. The entry of hashing table is calculated by direct mapping or XOR function to produce a 10-bit hashing address entry.

3.3.2 Learning Process

Address learning process is composed of source address (SA) of packets and hashing function. ADM5120 will compare the SA of each incoming packet:

a. If the source address of incoming packet is the same as the source MAC address table, then the aging status and port number will be updated.
b. If the source address is different from the source MAC address table (mean address collision), then no learning process will occur.

Exception cases of address learning:

1. The packets have error
2. The port learning is been disabled
3. Address collision
4. The source address is multicast
5. The packets from CPU

3.3.3 Routing

When a packet comes from portA, ADM5120 will compare its destination MAC address with the MAC address in the MAC address lookup table. If the address is the same and port number is portA means that the packet is a local packet, then it is discarded. If the address is the same but port numbers are different, the packet is a unicast packet, and will be forwarded to the assigned port. If the incoming packet is a broadcasted one, a multicast one, or an unknown one (i.e. the destination address cannot be found in the MAC address lookup table), then the routing scheme will broadcast it to all ports.
If the MAC address is VLAN address, then the packet will be routed to CPU port. The VLAN address is programmed by CPU, but not from the address learning.

3.3.4 Forwarding

ADM5120 provides store-and-forward method as forwarding scheme. Each outgoing packet, including to-CPU packets, will be stored in the buffer first, and then directly sent to the assigned port or CPU via DMA. However, only the good and non-local packets will be sent.

3.3.5 Buffer Management

The buffer memory is embedded in ADM5120 for the switch operations, which are designed based on output queuing and dynamic shared memory management architecture. It will assign buffer resources based on traffic status. In addition, this efficiency method can avoid the problem of Head-on-Line (HOL) blocking and cause better transmitting performance.

3.3.6 Flow Control (Patent Pending)

The on/off status for flow control depends on the global empty buffer count and per-port waiting-transmit count. Based on this intelligent scheme, if the packet transmits to the destination port that is full, then the flow control is turned on. And in the situation, the full condition is released, including packets transmitted out or disable, then the flow control is turned off.

ADM5120 does not do the flow control to CPU, mean – never send the flow control packets to CPU port, so the firmware needs to monitor the buffer status to prevent the packet lost.

3.3.7 Full Duplex

In full duplex flow control, ADM5120 follows IEEE 802.3x standards. If a PAUSE frame is received from a certain port, it will stop the port transmission of packets until the timer is timeout or another PAUSE frame with zero time is received. If the buffer is full and is in full-duplex mode, ADM5120 will send a PAUSE frame with the maximum value, to defer receiving packet. When enough buffer space is released, PAUSE frame with zero delay is sent.

3.3.8 Half Duplex

In half duplex operation, ADM5120 supports backpressure features. If free blocks in the buffer memory are below the threshold, a jam packet (jam mode) is sent to the connected segment, regardless of routing decisions.

3.3.9 Packet priority and Class of Service (CoS)

ADM5120 can set the packets as high priority as follows via registers:

Port Number
VLAN tag
TCP/IP TOS/DS
Customer defined type

The priority setting by port means that all the packets received by the port will be priority frames; ADM5120 can also judge the priority of frames by checking the specific bits of VLAN tag or TCP/IP TOS/DS in the frame or the customer defined type.

It will determine the packet priority. First it will check if the packet type meets VLAN or TCP/IP. Then, it will check whether the value of VLAN tag or TCP/IP TOS/DS field meets the registers setting. Depending on these two conditions, the scheme of weighted round robin can determine the high and low priority of frames, and thus set the transmitting order.

ADM5120 provides a function to improve the delay-time sensitive traffic in the flow-control condition. When the port receives a priority frame, the backpressure & 802.3x flow control can be turned off until no priority frame occurs within 1 or 2 seconds, then turned back on again (Patent Pending). So it can prevent the jitter caused by the flow control and the better timing-variation result for the priority traffic. This is a register programmable function.
All the packets from the CPU port will be treated as high priority for the switch ports, and then it can provide the best effort result for the CPU traffic (mostly they are this bandwidth is charged.)

3.3.10 VLAN

ADM5120 supports 7 port-grouping VLAN. Each of thr VLAN will be treated as the isolated ports.
ADM5120 provides the VLAN MAC address function, if the packet is assigned with the VLAN address as its destination MAC address, then this packet will be forwarded to the CPU via DMA.
For example, port0 is the WAN port, and the others are the LAN port, then WAN port set as VLAN1 and others set as VLAN2. And program the different MAC address for the VLAN1/2 into address table. Then if the LAN ports receive packets with VLAN2 addresses, the packets will be forward to the CPU via DMA. After processing the packets (like NAT), CPU can forward the packets to VLAN1.

3.3.11 Address table access

ADM5120 provides the access of the embedded MAC address.
Read - register B+48, 4C, and 50

Issue the search-start command, and ADM5120 will automatically search the embedded address table and report the valid one only.
If at the end of a table, it will also report the status.

Write - register B+58 and 5C

Fill the write address and other information, like port number (or VLAN number), age-time (or static), then issue the write command, and wait for the write done bit.

3.3.12 Address security

ADM5120 supports the source MAC address security function, register B+2C.
It can check all-incoming packets in the enable ports – compare the source MAC exists in the MAC address table or not, if not, discard the packets and report the status, register B+18.

3.3.13 Bandwidth control function

This is a patented feature of ADMtek.
ADM5120 can provide the RX/TX separated bandwidth control (or traffic shaping) function, which can be programmed to 64K- bit/ 128K /256K /512K/ 1M/ 4M/ 10M.
In a fixed period, ADM5120 will count the per port RX and TX byte number, and compare with the bandwidth control threshold. If it is over this threshold, ADM5120 will turn on the proprietary scheme to control the RX/TX behavior.

3.3.14 Send descriptors content

If CPU sends the packet to switch, either LAN or WAN, then the 'send descriptors' are used as follows:

Bit	Bit[31]	**Bit[28]**	Bit[24:0]	Remark
Type		control		Controlled by CPU
Function	Own bit	ring end flag	**buffer1_address**[24:0]	except Own-bit

Bit	Bit[31]	Bit[24:0]	Remark
Type	control		Controlled by CPU
Function	**buffer2_enable**	**buffer2_address**[24:0]	

Bit		Bit[10:0]	Remark
Type		control	Controlled by CPU
Function		**buffer1_length**[10:0]	

Bit	Bit[31]	Bit[26:16]	**Bit[13:8]**	**Bit[5:0]**	Remark
Type	Control				Controlled by CPU
Function	append_chksum	pkt-length [10:0]	**force desti-port[5:0]**	**To_VLAN[5:0]**	

Control

- Own bit:
  - If 0, the descriptor belongs to CPU. After the data is put in the buffer and control bits are set, this bit will change to 1 to indicate SW can process this packet.
  - If 1, the descriptor is for SW, and after the data is taken away, then it is loaded to SW data buffer, the bit will be then set to 0.
- Ring end: if 1, the descriptor is the last one, the next descriptor needs to return to the base address.
- Buffer information:
  - Each descriptor can support two buffers.
  - The buffer address can be any byte alignment.

  - Buffer1 has length information, if packet size is larger than buffer1 size, then get the rest of the data from buffer2.
  - Buffer address must be valid when a descriptor belongs to a switch, the switch engine will not check the address status.
  - Buffer2 has an enable bit to control whether the address is valid or not.
  - If the buffer2 is disabled and buffer1 is not long enough, then the remaining data will not be padded "0" to make the packet meet 64-bytes standard.
- append_chksum: need to append the IP (0x0800) and PPPoE (0x8864) packets IP-checksum by hardware
  - The packet checksum field must be pre-filled with all "0"'s
- Packet length: the packet length in bytes, excluding CRC if CRC is not padded. (See the register, CPUp_conf)
  - auto-padding: the engine can automatically pad the "0" into the packet which data size is less than 60B (or 64). The setting example: buffer 1 size=14, buffer 2 disable, the pkt length=60 (or 64 without CRC padding).
- Force desti-port[5:0]: the packet needs force forwarding to designated ports, and it is the highest priority of routing. If forced, then ignore the routing and To_VLAN flag.
- To_VLAN[5:0]: the bit-map, the packet forwards to the designated VLAN group. Use this flag to control the packets to LAN, WAN, or HPNA ports.

3.3.15 Receive descriptors content

If switch sends the packet to CPU, either LAN or WAN, then the 'receive descriptors' are used as follows:

Bit	Bit[31]	**Bit[28]**	Bit[24:0]	Remark
Type		control		Controlled by CPU
Function	Own bit	ring end flag	**buffer1_address**[24:0]	except Own-bit

Bit	Bit[31]	Bit[24:0]	Remark
Type	control		Controlled by CPU
Function	**buffer2_enable**	**buffer2_address**[24:0]	

Bit		Bit[10:0]	Remark
Type		control	Controlled by CPU
Function		**buffer1_length**[10:0]	

Bit	[26:16]	[14:12]		[5:4]	[3]	[2]	[1:0]	remark
Type	packet status							updated
function	pkt-length[10:0]	Source port number		00: UC 01: MC 10: BC	IP checksum fail	VLAN tag	00: 0x0800 01: 0x8864 11, 10: reserved	by switch

Control

- Own bit:
  - If 0, the descriptor belongs to CPU.
  - If 1, the descriptor is released to WAN MAC or LAN SW, which means it can store the incoming packet based on the buffer address. If this is done, change the bit to 0.
- Buffer information:
  - Each descriptor can support two buffers.
  - The buffer address can be any byte alignment.
  - Buffer1 has length information, if packet size is over the buffer1 size, then put the rest of the data into buffer2.
  - Buffer1 address must be valid when descriptor belongs to switch.
  - Buffer2 has a enable bit to control whether the address is valid or not.
  - The buffer2 size must be larger than the remaining data.
  - If buffer2 is disabled and buffer1 has not enough space, then the remaining data will be dropped, and no status reported.

Status

- Packet length: the packet length in bytes including 4-byte CRC
- Source port: the source port of packet
- DA status:
  - 00: UC, the packet is the forwarded UC packet
  - 01: MC, the packet has “1” in the LSB of first byte of DA
  - 11: BC, the packet has DA=FFFFFFFFFFFF
  - IP checksum fail: if 1 = the IP checksum result is error
    Note: Only checked if type = 0x0800(IP) or 0x8864(PPPoE)
- The VLAN tagged frame status (type=0x8100)
- Packet type:
  - 00: type = 0x0800, IP
  - 01: type = 0x8864, PPPoE
  - 10,11 reserved

3.4 USB 1.1 Host Controller

3.4.1 Block Diagram

The following block diagram describes the functional blocks of the ADMtek USB 1.1 Host controller.

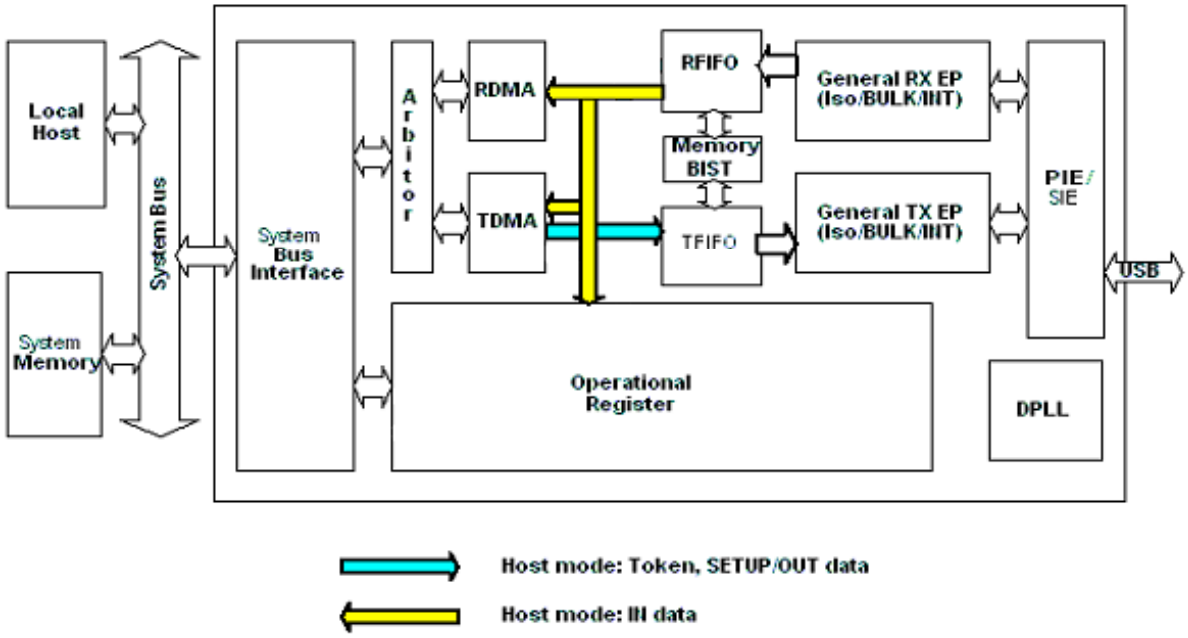


Figure 3-1 Block Diagram of ADMtek USB 1.1 Host controller

3.4.2 System bus interface

This block provides the USB Host controller with the connection to the AHB bus interface. The AHB bus is a 32-bit wide data bus, high-performance pipeline architecture. This block contains the AHB master interface and slave interface. Host can program the USB Host controller operational register via the AHB slave interface. The DMA units within the USB Host controller will act as bus masters and access the system memory through the AHB master interface.

3.4.3 Operational Register

This block is the CSR (configure and status register) of USB 1.1 Host controller. The local host configures USB 1.1 Host controller via these registers. It includes DMA, endpoint, enable/disable, and interrupt control. The local host gets the status of the USB 1.1 Host controller by reading the registers. It includes the DMA, interrupt and USB bus

status. The operational register also provides the interface for the local host to transfer the data for control and interrupt endpoint.

3.4.4 SIE

The SIE handles the link layer protocol of USB. It includes the following items

- Identify the USB SYNC field
- Identify the USB address, endpoint field
- Decode/encode the NRZI
- Generate/check the Bit Stuffing and the CRC
- Convert the USB incoming serial data to 8-bit parallel data
- Convert 8-bit parallel data to USB serial data
- Detect/report/generate USB bus events such as Reset, Suspend and Resume

3.4.5 DPLL

The DPLL block is a digital phase lock loop for extracting clock and data from the USB bus

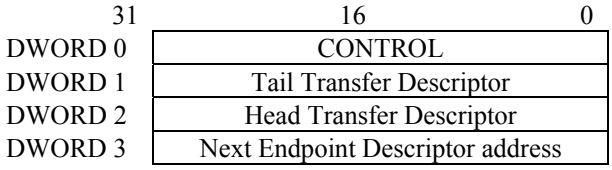
3.4.6 Memory BIST

The Memory BIST block is used for testing TFIFO and RFIFO. In this memory BIST, the MARCH C- test algorithm is adopted and the test data bus is 32-bits in width for each FIFO block. During the test period, all FIFO blocks are tested concurrently and the test procedure will be aborted if any fault is detected.

3.5 DMA Operation

4 kinds of Endpoints data transfer (Control, Interrupt, Bulk and Isochronous) are supported in host mode.

3.5.1 Endpoint Descriptor Format



DWORD 0 – Control

Bit	Description
31-27	**Reserved**
26-16	**Maximum packet size** The maximum data that can transmit/receive in one USB transaction.
15	**Format** This bit indicates that this packet is for isochronous. 1: The data in this descriptor is for isochronous transfer. 0: The data in this descriptor is for general data transfer.
14	**Skip** When this bit is set, DMA will continue on the next descriptor in the link list, this is used for isochronous and periodic data transmission/reception.
13	**Speed** This bit indicates that the speed of the data transfer.
12	**Reserved**
11	**INT** This bit indicate this ED is an interrupt endpoint
10-7	**EN** Endpoint number of the current USB function.
6-0	**FA** Function address of the current USB device.

DWORD 1 – Tail Transfer Descriptor

Bit	Description
31-4	**Starting address of the tail transfer descriptor in host memory space**
3-0	**Reserved**

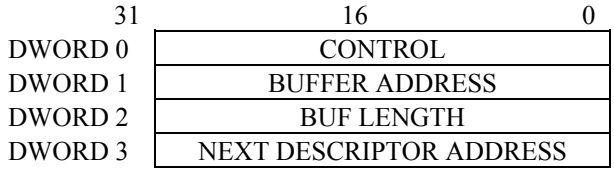
DWORD 2 – Head Transfer Descriptor

Bit	Description
31-4	**Starting address of the head transfer descriptor in host memory space**
3-2	**Reserved**
1	**Togglecarry** This bit indicate the current toggle value in this transaction.
0	**Halt** This bit indicates that this endpoint is halted due to error.

DWORD 2 – Next Endpoint Transfer Descriptor

Bit	Description
31-4	**Starting address of the next endpoint transfer descriptor in host memory space**
3-0	**Reserved**

3.5.2 Transfer Descriptor Format



DWORD 0 – Status

Bit	Description
31	**OWNER** Descriptor ownership bit – set to 0 when the host owns the descriptor, set to 1 by host to tell the USB Host controller owns the descriptor, the controller will clear this bit when reception has done.
30-27	**Complete code** The transfer status of each USB transfer. 4'b0000 : No Error. 4'b0001 : CRC Check Error. 4'b0010 : Bit-Stuffing Error. 4'b0011 : Data Toggle Error. 4'b0100 : STALL. 4'b0101 : Device No Response (Timeout). 4'b0110 : PID Error (Invalid PID). 4'b0111 : Unexpected PID. 4'b1000 : Data Overrun (Packet Overrun). 4'b1001 : Data Underrun (Packet Underrrun). 4'b1100 : Buffer Overrun. 4'b1101 : Buffer Underrrun.
26-25	**EC** Error count thet error that happens at each of USB transfer.
24-23	**Toggle(Data Toggle bit)** Data toggle bit. This field is used for data PID value. 24: when 0, use togglecarry bit in ED as the PID when 1, use but 23 as the toggle bit. 23: toggle value
22-21	**DIR** These bits indicate this packet's direction. 00: SETUP packet 01: OUT packet. 10: IN packet. 11: reserved
20-14	**Reserved**
13-8	**Interrrupt service interval** This field indicate the frame interval that the interrupt transaction occurs. The frame interval = bit [13:8] + 1
7-6	**Reserved**
5-0	**Frame number** This field indicate the frame number that receive/transmit this data, this field is only valid when configurated in Isochronous and interrupt transaction. For Isochronous transaction, it indicates the frame number in which the isochronous transaction should occur. For interrupt transaction, software use this field to indicate to hardware for the "starting frame number" of the interrupt transaction, hardware will update this field to the "next frame number" after the current transaction is done.

DWORD 1 – Data Buffer Pointer

Bit	Description
31-0	**Starting address of the data buffer** This field indicates the starting address of the data buffer. Data buffer may be aligned on any byte. When an OUT or SETUP packet has been transmitted, this field will be updated as the next start address of the data buffer.

DWORD 2 – CONTROL/BUF Length

Bit	Description
31-17	**Reserved**
16	**Interrupt enable** This field indicates that whether the interrupt will be asserted when this descriptor is completed.
15-0	**Length of data buffer** This field indicates the length of the current data buffer.

DWORD 3 – Next Transfer Descriptor Pointer

Bit	Description
31-4	**Starting address of the next descriptor in host memory space**
3-0	**Reserved**

3.5.3 DMA operation

To provide a high-performance and effective way for software packet scheduling, the DMA is able to handle both transmit and receive packets in a single descriptor chain. In the endpoint and transfer descriptors, the software can specify the descriptor format (Isochronous or none-Isochronous), direction, speed, and data toggle bit.

If there is any isochronous or periodic data that needs to be transmitted/received, this descriptor needs to link at the beginning of the link list to guarantee the bus bandwidth. After these descriptors, the control or bulk descriptor is linked.

DMA starts to access the first descriptor in the link list and transmit/receive the data through the USB bus. Since there might be several USB packets segmented in one descriptor. After one USB packet is transmitted, DMA will update the **transmit status**, **data length**, **start address of the data buffer**, and **length of data buffer** for further access, and advance to the next descriptor.

When the DMA finishes it's transmit/receive of a descriptor, it depends on the setting of the **interrupt enable** to generate HC_INT to indicate this descriptor is ready for the software driver process.

If all the descriptors have been accessed once, and the frame is not yet over, then the DMA will try to access the general descriptor again in order to get a high performance.

If a USB zero length packet is received, then the received data length will be zero, and this buffer is retired due to short packet received.

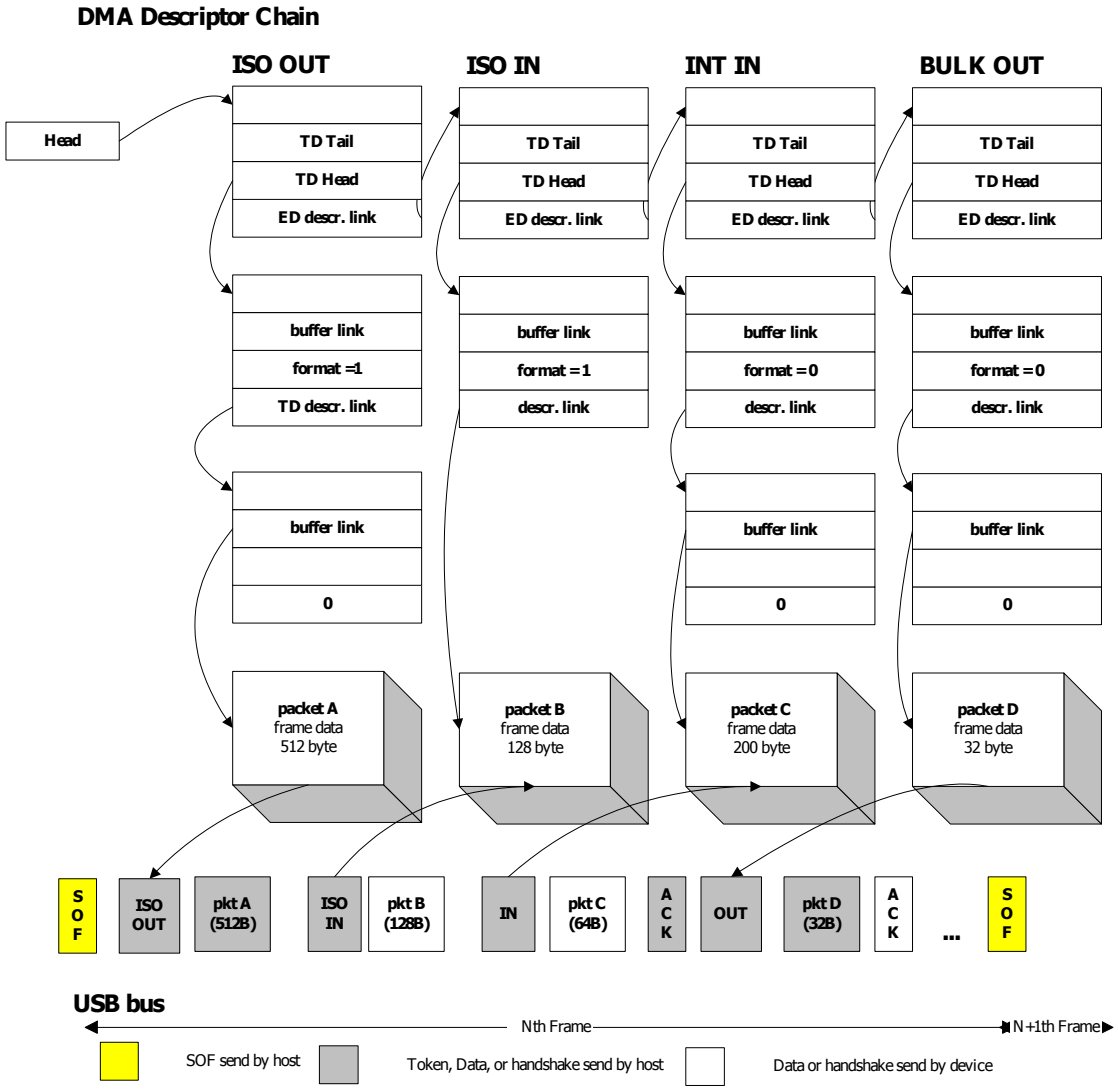


Figure 3-2 DMA Operation in Host mode

For Interrupt IN/OUT transactions, each ED just contains one valid TD. Since the Interrupt transaction is periodic, two parameters are defined in TD by software to guide hardware for doing Interrupt transfer, they are Frame Number and Interrupt service period. The Frame Number is used by the software to indicate the frame number of which the first Interrupt transaction occurs, of this TD. The Interrupt service period indicates the frame interval between the current Interrupt transaction and the next one, Frame_Interval is calculated by the following formula:

Frame_Internal = (Interrupt service period + 1)

The transfer of interrupt transaction is activated just when the current frame number matches the Frame Number of the TD, after the current transaction is served, the next frame number will be updated to TD descriptor by hardware, then the hardware waits for the next matched frame number to serve the Interrupt transaction, and so on. . The next Frame Number is calculated by (current_Frame_Number) + Frame_Interval. The following diagram describes how Frame_Number and Interrupt_service_period work.

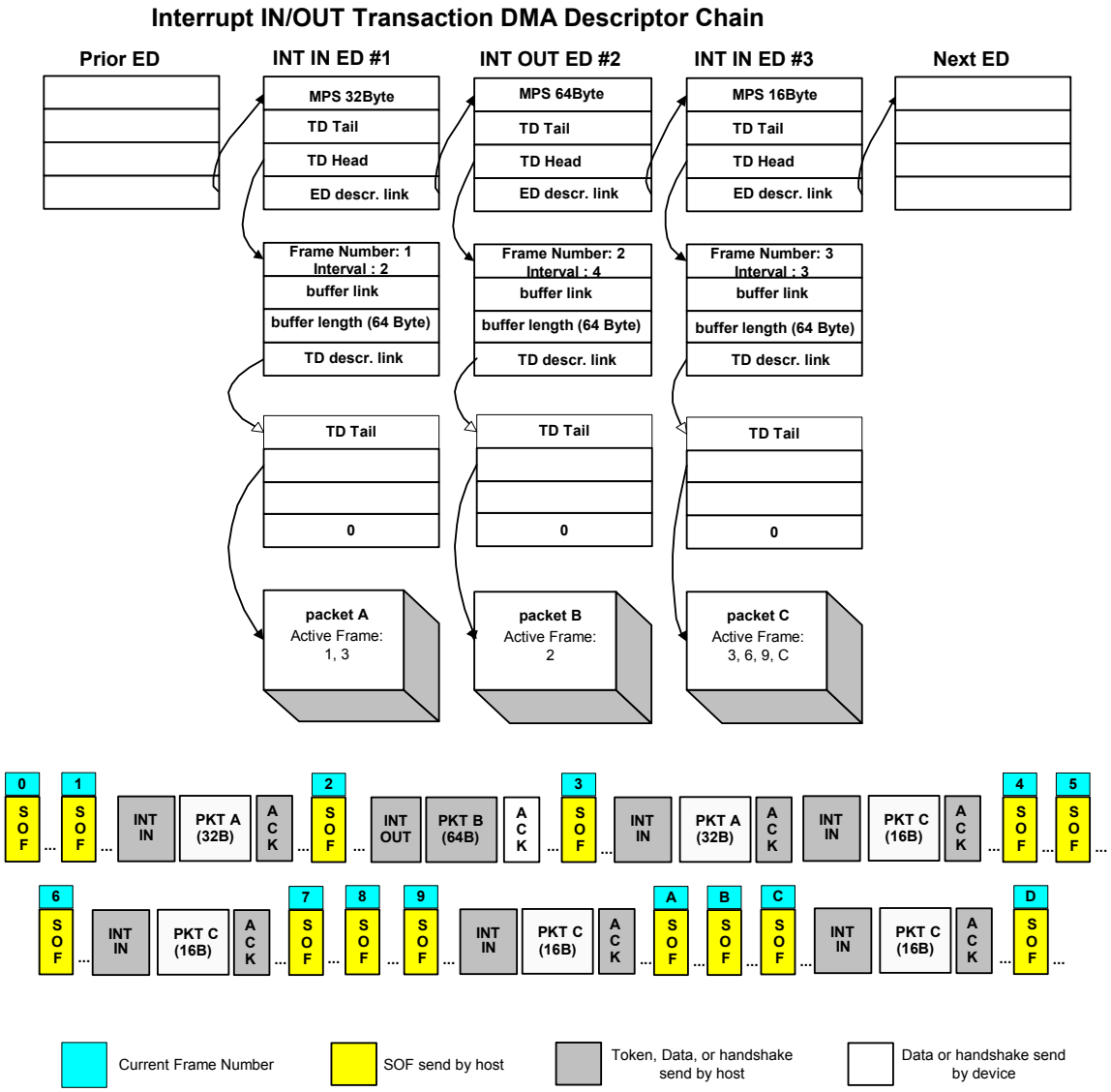


Figure 3-3 Interrupt IN/OUT Transactions

Chapter 4 Register Description

4.1 System Memory Map

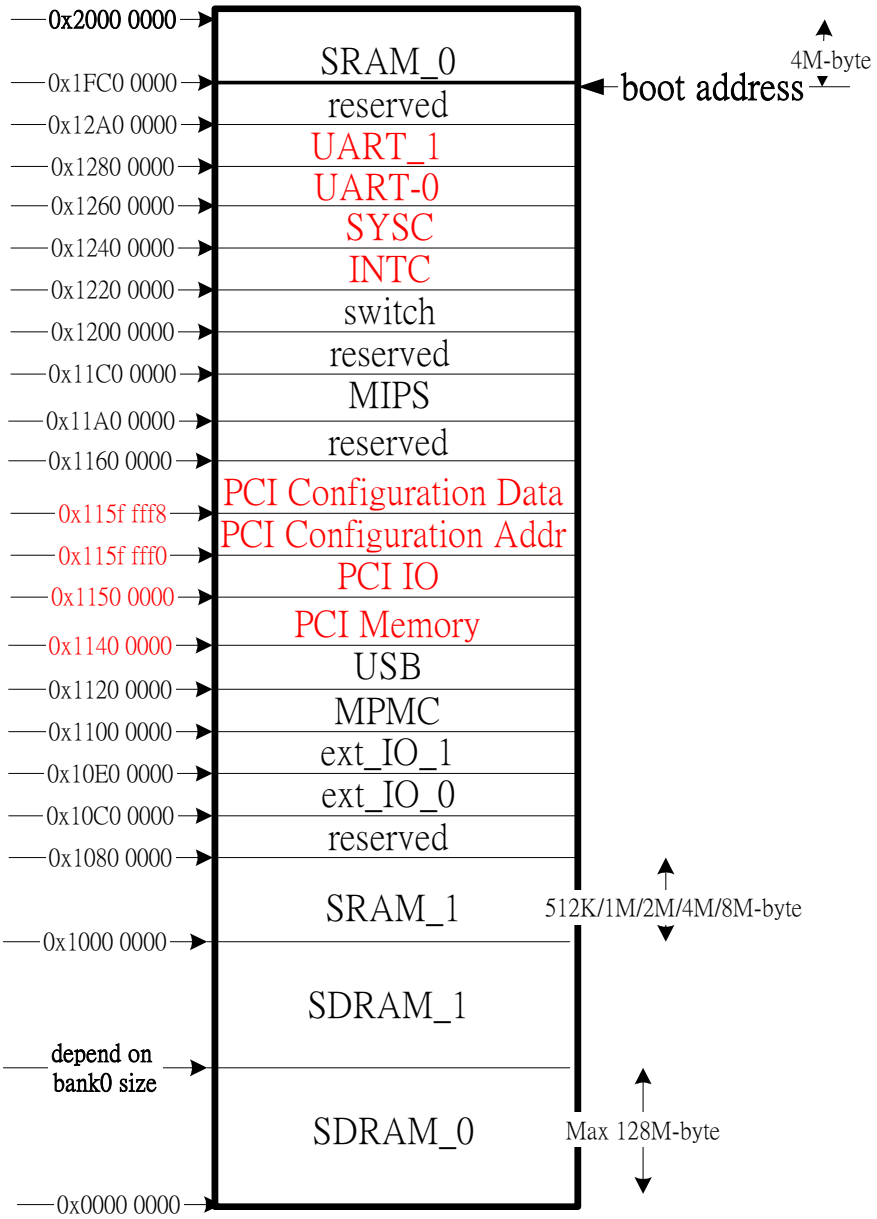


Figure 4-1 System Memory Map

SYSC: System control registers
INTC: INTERRUPT CONTROL REGISTERS

Memory mapping notes

- There are two banks for SDRAM and Flash.
- The two banks of SDRAM are the same size.
  - control register, Base+1C, bit[2:0]
- For SRAM
  - SRAM_0, the bank0of NOR flash, boot flash
    - the address is fixed at 0x1FC0_0000 and the maximum size is 4M-byte.
    - If in the NOR type mode, the data-width is pin setting and register readable. The size is programmable.
  - SRAM_1, the bank1 of NOR or NAND flash
    - The address is fixed at 0x1000_0000
    - The maximun size is 8M-byte. The size is programmable.
    - If in the NAND type mode, no SRAM_0 device. The boot code will load into the embedded SRAM from NAND flash in the initial time.
  - all the data-width information as ➔
    - byte access, address=[20:0], max size=2M bytes
    - 16-bit access, address=[21:1] (shift A0 out), max size=4M bytes
    - 32-bit access, address=[22:2] (shift A0, A1 out), max size=8M bytes
    - use DQM to select the bytes
- PCI device
  - 0x1140_0000 to 0x114f_ffff is PCI memory access
  - 0x1150_0000 to 0x115f_ffef is PCI I/O space
  - 0x115f_fff0 is PCI configuration address port (Dword Access only)
  - 0x115f_fff8 is PCI configuration data port(Dword Access only)

Design notes

- PCI device
  - PCI_Device_ID : 5120h
  - PCI_Vendor_ID : 1317h
  - PCI_Class_Code : 060000h
  - PCI_Revision_ID : 00h
  - PCI_Subsystem_ID : 0000h
  - PCI_Subsystem_Vendor_ID : 0000h
  - AHB to PCI Bridge IDSEL is PCI_AD[11] external PCI device's IDSEL can use PCI_AD[12] or higher bits.
- Pause Frame must meet all of the following spec.
  - Right DA: DA=0180c2000001 or unicast MAC address belong to CPU
  - Right type field = 8808
  - Right op-code = 0001
  - Right CRC

4.2 System and Interrupt Registers

4.2.1 Interrupt Control Register Map

Offset Address	**name**
Base + 00	**IRQ_status**
Base + 04	**IRQ_raw_status**
Base + 08	**IRQ_enable**
Base + 0c	**IRQ_enable_clear**
Base + 10	**Reserved**
Base + 14	**INT_mode**
Base + 18	**FIQ_status**
Base + 1c	**IRQ_test_source**
Base + 20	**IRQ_source_sel**
Base + 24	**INT_level**

Note: Base = 0x1220_0000

4.2.2. Interrupt Request Source Description

Bit	Name	Description
[9]	Sw_int	Switch interrupt, refer to B+B0, B+B4
[8]	PCI 2	PCI INT2
[7]	PCI 1	PCI INT1
[6]	PCI 0	PCI INT0
[5]	Intx_1	Internal interrupt 1, refer to GPIO[4] is the source
[4]	Intx_0	Internal interrupt 0, refer to GPIO[2] is the source
[3]	USB	USB interrupt source
[2]	UART1	UART1 interrupt source
[1]	UART0	UART0 interrupt source
[0]	timer	Timer interrupt, refer to B+F0 and B+F4

Note: Only support level sensitive interrupts.
The external interrupt level, active high or low can be programmed

4.2.3 IRQ_status, offset: 0x00

Bits	Type	Name	Description	Initial value
9:0	RO	IRQ_status[7:0]	The status of the interrupt sources **after** masking. 1: the corresponding IRQ is active, and generate the interrupt to MIPS	0
31:10	RO	Reserved		0

4.2.4 IRQ_raw_status, offset: 0x40

Bits	Type	Name	Description	Initial value
9:0	RO	IRQ_raw_status[7:0]	The status of the interrupt sources **before** masking. 1: the corresponding IRQ is active	0
31:10	RO	Reserved	Not Applicable	0

4.2.5 IRQ_enable, offset: 0x80

Bits	Type	Name	Description	Initial value
9:0	RW	IRQ_enable[7:0]	The enable register is used to mask the interrupt source. 1: enable the interrupt and allow the interrupt request to MIPS. Writing “0” has no effect.	0
31:10	RO	Reserved	Not Applicable	0

4.2.6 IRQ_enable_clear, offset: 0xc0

Bits	Type	Name	Description	Initial value
9:0	RW	IRQ_enable_clear [7:0]	The clear bits of the IRQ_enable. Writing “1” clear the corresponding bit of IRQ_enable. Writing “0” has no effect.	0
31:10		Reserved	Not Applicable	

4.2.7 Reserved, offset: 0x10

Bits	Type	Name	Description	Initial value
31:0		Reserved	Not Applicable	

4.2.8 INT_Mode, offset: 0x14

Bits	Type	Name		Initial value
9:0	RW	INT_mode[9:0]	The interrupt type of the interrupt sources . 1: the corresponding Interrupt port generate the FIQ to MIPS 0: the corresponding Interrupt port generate the IRQ to MIPS	0
31:10		Reserved	Not Applicable	

4.2.9 FIQ_status, offset: 0x18

Bits	Type	Name		Initial value
9:0	RW	FIQ_status[9:0]	The status of the fast interrupt sources **after** masking. 1: the corresponding IRQ is active, and generate the interrupt to MIPS	0
31:10		Reserved	Not Applicable	

4.2.10 IRQ_test_source, offset: 0x1c

Bits	Type	Name		Initial value
9:0	RW	IRQ_test_source[9:0]	the test data for the IRQ_raw_status	0
31:10		Reserved	Not Applicable	

4.2.11 IRQ_source_sel, offset: 0x20

Bits	Type	Name		Initial value
0	RW	IRQ_source_selection	1: load the IRQ_test_source into IRQ_raw_status	0
31:1		Reserved	Not Applicable	

4.2.12 INT_level, offset: 0x24

Bits	Type	Name		Initial value
3:0	RO	Reserved	Not Applicable	
8:4	RW	INT_level	external interrupt source 0: active high (default) 1: active low	0
31:1		Reserved	Not Applicable	

4.3 Switch Control Register Map

Note: Base = 0x1200_0000

Description	Offset	Type*	Page Number
Code	0x00	RO	4-5
SftReset	0x04	WO	4-6
Reserved	0x08		4-6
SWReset	0x0c	WO	4-6
Global_St	0x10	RO	4-6
PHY_St	0x14	RO	4-7
Port_St	0x18	RO	4-7
Mem_cRWontrol	0x1c	RW	4-8
SW_conf, offset:	0x20	RW	4-8
CPUp_conf	0x24	RW	4-10
Port_conf0	0x28	RW	4-10
Port_conf1	0x2c	RW	4-11
Port_conf2	0x30	RW	4-11
Reserved	0x34		4-12
Reserved	0x38		4-12
Reserved	0x3c		4-13
VLAN_GI	0x40	RW	4-13
VLAN_GII	0x44	RW	4-13
Send_trig	0x48	RW	4-13
Srch_cmd	0x4c	RW	4-13
ADDR_st0	0x50	RO	4-14
ADDR_st1	0x54	RO	4-14
MAC_wt0	0x58	RW	4-14
MAC_wt1	0x5c	RW	4-14
BW_cntl0	0x60	RW	4-15
BW_cntl1	0x64	RW	4-15
PHY_cntl0	0x68	RW	4-15
PHY_cntl1	0x6c	RO	4-16
FC_th	0x70	RW	4-16
adj_port_th	0x74	RW	4-16
Port_th	0x78	RW	4-16
Reserved	0x7c		4-16
Reserved	0x80		4-17
Pri_cntl	0x84	RW	4-17
VLAN_pri	0x88	RW	4-17
TOS_en	0x8c	RW	4-18
TOS_map0	0x90	RW	4-18

TOS_map1	0x94	RW	4-18
Custom_pri1	0x98	RW	4-18
Custom_pri2	0x9c	RW	4-18
Reserved	0xA0		4-19
Empty_cnt	0xA4	RO	4-19
Port_cnt_sel	0xA8	RW	4-19
Port_cnt	0xAc	RO	4-19
Int_st	0xB0	RW	4-20
Int_mask	0xB4	RW	4-21
GPIO_conf0	0xB8	RW	4-22
GPIO_conf2	0xBc	RW	4-22
Watchdog0	0xC0	RW	4-22
Watchdog1	0xC4	RW	4-22
Swap_in	0xC8	RW	4-23
Swap_out	0xCc	RO	4-23
send_Hbaddr	0xD0	RW	4-23
send_Lbaddr	0xD4	RW	4-23
receive_Hbaddr	0xD8	RW	4-23
receive_Lbaddr	0xDc	RW	4-24
send_Hwaddr	0xE0	RO	4-24
send_Lwaddr	0xE4	RO	4-24
receive_Hwaddr	0xE8	RO	4-24
Receive_Lwaddr	0xEc	RO	4-24
Timer_int	0xF0	RW	4-24
Timer	0xF4	RW	4-25
Reserved	0xF8		4-25
Reserved	0xFc		4-25
port0_LED	0x100	RW	4-25
port1_LED	0x104	RW	4-25
port2_LED	0x108	RW	4-25
port3_LED	0x10c	RW	4-26
port4_LED	0x110	RW	4-26

Note: Although some registers may be marked with a certain type, it may be possible that some bits in this register are different. This is explained in the register description.

4.4 Switch Control Register Description

4.4.1 Code, offset: 0x00

Bits	Type	Name	Description	Initial value
15:0	RO	Product Code	Product code = 0x5120(Hex)	0x5120h

19:16		Revision	Revision code = 1000 (5120)	
21:20		Clock_spd	The PLL setting: 00: 175MHz (Default) 01: 200MHz 1x: Reserved	00
24		NAND boot	Configured in the NAND flash boot	
25		Dcache_Set	1: 2K per way. 0: 4K per way	
26		Dcache_Size	1: 2 Ways. 0: 1 Way.	
27		Icache_Set	1: 2K per way. 0: 4K per way	
28		Icache_Size	1: 2 Ways. 0: 1 Way.	
29		Package	0: BGA. 1: 208PQFP/disable GMII	
31:30		Reserved	Not Applicable	

4.4.2 SftReset, offset: 0x04

Note: Whenever you write the register offset 0x04, the SftReset will be active.

Bits	Type	Name	Description	Initial value
	WO	SftReset	Do Software reset when write, reset all logic, PHY and memory, and down load the NAND flash content again. Same as hardware reset.	

4.4.3 Boot_done, offset: 0x08

Bits	Type	Name	Description	Initial value
0	RW	Reserved	1: the software boot process is done and the address table can return to switch controller	

4.4.3 SWReset, offset: 0x0c

Note: Whenever you write the register offset 0x04, the SWReset will be active.

Bits	Type	Name	Description	Initial value
	WO	SWReset	Do SW reset when write, including SW engine, data-buffer, link table, and PHY excluding address table. (Recommend stop PHY before reset switch)	

4.4.5 Global_St, offset: 0x10

Bits	Type	Name	Description	Initial value

0	RO	D_bist_fail	Data buffer BIST result → 0: Pass	
1	RO	L_bist_fail	Link table BIST result → 0: Pass	
2	RO	MC_bist_fail	MC table BIST result → 0: Pass	
3	RO	AT_bist_fail	address table BIST reseult → 0: Pass	
5:4	RO	Dcache_D_test_fail	Bit 5 and Bit 4 are respectively for the upper and lower 32-bit of D-cache memory for data → 00: Pass	
6	RO	Dcache_T_test_fail	the memory of D-cache tag → 0: Pass	
8:7	RO	Icache_D_test_fail	Bit 8 and Bit 7 are respectively for the upper and lower 32-bit of I-cache memory for data → 00: Pass	
9	RO	Icache_T_test_fail	the memory of I-cache tag → 0: Pass	
10	RO	all_mem_test_done	all embedded memory test completed → 1: complete	
19:11	RO	skip_blocks	the number of block is skipped up to 64 blocks	
21	RO	Dcache_portion	For debugging purpose of embedded SRAM	
22	RO	Icache_portion	For debugging purpose of embedded SRAM	
31:23		Reserved	Not Applicable	

4.4.6 PHY_St, offset: 0x14

Bits	Type	Name	Description	Initial value
4:0	RO	Link	PHY Link→ 1=up, 0=down	
5	RO	MII_fail	MII_fail → MII, 1=link ok, 0= port fail	
7:6		Reserved	Not Applicable	
12:8	RO	Speed	Speed→ 1=100M, 0=10M	
14:13		GMII_speed	GMII port speed → 10: giga(disable on PQFP), 01:100M, 00: 10M	
15		Reserved	Not Applicable	
21:16	RO	Duplex	Duplex→ 1= full duplex, 0=half duplex	
23:22		Reserved	Not Applicable	
28:24	RO	FC_st	FC → 1 = full duplex and 802.3x flow control ON (after AN or forced)	
30:29		GMII_FC_st	FC status of GMII port → [29]=1, FC on if 10/100M, RX_FC on if giga, [30]=1, TX_FC on if giga	
31		Reserved	Not Applicable	

4.4.7 Port_St, offset: 0x18

Bits	Type	Name	Description	Initial value
5:0	RO	Secured_st	Security status → 1= has intruder coming if turn on the SA_securd mode	
6		Reserved	Not Applicable	
7	RO	TXC_st	TXC_st→ MII port TXC status, 1= error, no TXC or too long period	
31:8		Reserved	Not Applicable	

4.4.8 Mem_control, offset: 0x1c

Bits	Type	Name	Description	Initial value
2:0	RW	SDRAMsize	one bank information, the 2nd bank (SDRAM_CS1) is the same 000, 101, 110, 111: reserved, 001: 1Mx32 (4Mbyte), 010: 2Mx32 (8Mbyte) (suggested setting) 011: 4Mx32 (16Mbyte), 100: 16Mx32 (64Mbyte) 101: 32Mx32 (128Mbyte)	
4:3		Reserved	Not Applicable	
5	RW	SDRAM1_en	The bank1 of SDRAM enable, 0: disable (default), 1: enable (must in the single write)	0
7:6		Reserved	Not Applicable	
10:8	RW	SRAM0_size	000: disable if in the NAND mode, 110, 111: reserved, 001: 512Kbyte, 010: 1Mbyte (default) 011: 2Mbyte, 100: 4Mbyte	010
15:11		Reserved	Not Applicable	
18:16	RW	SRAM1_size	000: disable (default), 001: 512Kbyte, 010: 1Mbyte 011: 2Mbyte, 100: 4Mbyte, 101: 8Mbyte, 110, 111: reserved	000
28:19		Reserved	Applicable	
29	RW	CSX0_wt_hold_ext	Extend the write data hold time from one clock to 3 clock (clock period = CLK_OUT) 0: normal, 1 clock, default, 1: extend to 3 clocks	1
31:30		Reserved	Not Applicable	

4.4.9 SW_conf, offset: 0x20

Bits	Type	Name	Description	Initial value
0		Reserved	Not Applicable	0
3:1		Reserved	Not Applicable	
7:4	RW	age_tmr	aging timer → 0000: disable age, 1xxx: fast age 0001: 300sec, 0010: 600 …… 0111: 38400sec	0001
9:8	RW	BC_prev	Broadcast prevention:	00

Bits	Type	Name	Description	Initial value
			00: disable, BC will be blocked, if 01=64 blocks 10=48 blocks 11=32 blocks	
11:10	RW	Max_len	Maximum packet length: 00: 1536, 01: 1518, 10: 1522, 11: reserved	00
12	RW	Dis_colabt	1: Disable collision 16 packet abort	
14:13	RW	Hash_alg	MAC address hashing algorithm: 00: direct mode, using last 10-bit as hashing address 01: XOR48 mode 10: XOR32 mode, 11:reserved	00
15	RW	force_bk	Disable the collision back off timer: 1: re-transmit immediately after collision, 0: follow standard	0
19:16	RW	BP_num	Back pressure jam number: the consecutive jam time when back pressure, Default = 1010, 10 packet jam then one no-jam	1010
21:20	RW	BP_mode	Back pressure mode : 00: disable 01: BP jam, the jam number is set by BP_num 10: BP jamALL, jam packet until the BP condition is released (default), 11: BP carrier, use carrier insertion to do back pressure	10
22	RW	Rsrv_MC	Reserved MC filtering: 1: filtered, 0: forwarded Note: Reserved MC = 01-80-c2-00-00-00 (BPDU) and 01-80-c2-00-00-02 to 01-80-c2-00-00-0f	0
23	RO	BISR_disable	Build-in self repair disable → 0: enable skip function (default, from pin A[5])	0
24	RW	disMII_wasTX	MII0 port disable was_transmit: 1: disable was_transmit (good for late CRS PHY, like HPNA2.0 or power-LAN), 0: enable	0
25	RW	BISS_disable	Build-in self skip disable: 0 = enable skip function (default, from pin A[6])	0
27:26	RW	BISS_TH	The threshold of BISS: 00:skip if fail 16 (default, from pins) 01:skip if fail 48 10:skip if fail 64 11:skip if fail 8 blocks	00

Bits	Type	Name	Description	Initial value
31:28	RW	Req_lat	AHB request latency = the AHB bus request latency, 4: 4 clocks latency between requests	

4.4.10 CPUp_conf, offset 0x24

Bits	Type	Name	Description	Initial value
0	RW	DisCPUport	Disable CPU port = 1: disable the switch CPU port, and so send packets to CPU and clear all the packets in the switch buffer	1
1	RW	CRC_padding	CRC padding from CPU = 1: the packet from CPU with CRC	0
2	RW	bridge mode	bridge testing mode: 0: default 1: forward to CPU, if the DA is the port, belonged to the other VLAN (for the bridge mode testing)	0
8:3		Reserved	Not Applicable	
14:9	RW	DisUN_port	Disable unknown packets, from port(s), forward to CPU → 1: no send unknown packet from the port0 to port5 to CPU	
15		Reserved	Not Applicable	
21:16	RW	DisMC_port	Disable multicast packets, from port(s), forward to CPU → 1: no send MC from the port0 to port5 to CPU	
23:17		Reserved	Not Applicable	
29:24	RW	DisBC_port	Disable broadcast packets, from port(s), forward to CPU → 1: no send BC from the port0 to port5 to CPU	
31:30	RW	Reserved	Not Applicable	

4.4.11 Port_conf0, offset 0x28

Bits	Type	Name	Description	Initial value
5:0	RW	Dis_port	Disable port → 1: port disable (if dumb mode, default = 0)	
7:6		Reserved	Not Applicable	
13:8	RW	En_MC	enable all MC packet broadcast to port in the same VLAN (**not including CPU**) → 1: enable Layer2 MC broadcast to ports, 0: do not broadcast MC	
15:14		Reserved	Not Applicable	
21:16	RW	En_BP	Enable back pressure → 1: enable back pressure (but need qualify BP_mode)	

4.4.12 Port_conf1, offset 0x2c

Bits	Type	Name	Description	Initial value
5:0	RW	Dis_Learn	Stop SA learning → 0: enable SA learn	
11:6	RW	blocking_state	blocking state, only do the forwarding to CPU, and no learning, and no transmitting (except the packet from CPU) → 0: normal state, 1: block state	
17:12	RW	blocking_mode	If in blocking state → 1: only forward control packets to CPU, 0: forward all packets to CPU	
19:18		Reserved	Not Applicable	
25:20	RW	Port_age	port aging: 1: enable aging, 0: disable aging that the MAC address is belong to programmed port(s)	1
31:26	RW	SA_secured	SA secured mode: 0: don't care SA match, 1: the pakcets' SA need match, otherwise discard the packets ***Note***: 1. set Dis_Learn and SA_secured at the same time, then only forward the packets with the SA and port number matched. 2. 2. set SA_secured only, then no any secured function	

4.4.13 Port_conf2, offset 0x30

Bits	Type	Name	Description	Initial value
0	RW	GMII_AN	MII port AN monitor enable: 1: enable MII AN monitor via MDIO (if in the dumb mode, set to 1), 0: disable	0
2:1	RW	force_MIIport_spd	Force MII port speed if AN monitor disable: 00: forced in 10M 01: forced in 100M 10: forced in giga 11: reserved	
3	RW	force_MIIport_dpx	Force MII port duplex if AN monitor disable: 0: forced in half duplex 1: forced in full duplex. Note: duplex is forced in full, if speed is forced in the giga	
5:4	RW	force_MIIport_FC	Force MII port 802.3x flow control ON if AN monitor disable: 00: no forced,	0

Bits	Type	Name	Description	Initial value
			bit[4]=1, forced the FC of 10M/100M, forced the RX FC of giga, bit[5]=1, forced the TX FC of giga	
6		Reserved	Not Applicable	
7	RW	rev-MII	0: normal MII mode (default), 1: reversed MII if MII enable and only in the 10M/100M speed, and only in the AN monitor disable reversed MII mode (AN will be off) – drive TXC, RXC, COL, and CRS (5120 side) RXC → RXC (MAC side) TXC → TXC TXD → RXD TXE → RXDV RXD ← TXD RXDV ← TXE COL → COL CRS → CRS 1: enable(if in the dumb mode, set to 1),	0
8	RW	TXC_check	check the MII port TXC period, if more than 400us, then disable MII port 1: disable, check TXC(only for 10/100M)(default) 0: enable check.	1
10:9	RW	Config_early_rdy[1:0]	Giga Port early preamble configuration. Default value 00	0
15:11		Reserved	Not Applicable	
17:16	RW	LED_flash_time	The frequency of LED flash: 00: 30ms, 01: 60ms, 10: 240ms, 11: 480ms	00
23:18		dis_uc_pause[5:0]	Disable unicast pause frame. Default 00000.	
31:24		Reserved	Not Applicable	

4.4.14 Reserved, offset: 0x34

Bits	Type	Name	Description	Initial value
		Reserved	Not Applicable	

4.4.15 Reserved, offset: 0x38

Bits	Type	Name	Description	Initial value
		Reserved	Not Applicable	

4.4.16 Reserved, offset: 0x3c

Bits	Type	Name	Description	Initial value
		Reserved	Not Applicable	

4.4.17 VLAN_GI, offset 0x40

Bits	Type	Name	Description	Initial value
6:0	RW	VLAN0	VLAN group 0 → the ports in VLAN group0, the 6th bit is CPU port 1111111: ALL PORTS IN THE VLAN GROUP0	1111111
7		Reserved	Not Applicable	
14:8	RW	VLAN1	VLAN group 1 → the ports in VLAN group1, 0000000	0000000
15		Reserved	Not Applicable	
22:16	RW	VLAN2	VLAN group 2 → the ports in VLAN group2, 0000000	0000000
23		Reserved	Not Applicable	
30:24	RW	VLAN3	VLAN group 3 → the ports in VLAN group3, 0000000	0000000
31		Reserved	Not Applicable	

4.4.18 VLAN_GII, offset 0x44

Bits	Type	Name	Description	Initial value
6:0	RW	VLAN4	VLAN group 4 → the ports in VLAN group4, 0000000	0000000
7		Reserved	Not Applicable	
14:8	RW	VLAN5	VLAN group 5 → the ports in VLAN group5, 0000000	0000000
31:15		Reserved	Not Applicable	

4.4.19 Send_trig, offset 0x48

Bits	Type	Name	Description	Initial value
0	RW	Send_trig_L	CPU Send packet to LAN/WAN DMA trigger (normal priority), self_clear	
1	RW	Send_trig_H	CPU Send packet to LAN/WAN DMA trigger (high priority), self_clear	
31:2		Reserved	Not Applicable	

4.4.20 Srch_cmd, offset 0x4c

Bits	Type	Name	Description	Initial value
0	RW	Srch_start	searching from the start of address table, self_clear	
1	RW	Srch_again	search for the next available address, self_clear (program again after data_rdy)	
31:2		Reserved	Not Applicable	

4.4.21 ADDR_st0, offset 0x50

Bits	Type	Name	Description	Initial value
0	RO	Data_rdy	Data is ready → ADDR_st, ADDR_srch0 and ADDR_srch1 are ready, read_clear	
1	RO	Table_end	Search to table end → 1: hit the end of MAC address table	
2	RO	filter	Filter bit	
5:3	RO	VLAN	VLAN number	
6	RO	VLAN_en	VLAN field is enable	
12:7	RO	P_number	Port number (refer to B+58, bit7-4)	
15:13	RO	age_field	Age-field: 000 empty 001 to 110 existed MAC, 111 static address,	
31:16	RO	MAC_srch0	MAC address [15:0]	

4.4.22 ADDR_st1, offset 0x54

Bits	Type	Name		Initial value
31:0	RO	MAC_srch1	MAC address [47:16]	

4.4.23 MAC_wt0, offset 0x58

Bits	Type	Name	Description	Initial value
0	RW	wtMAC_cmd	MAC address write command → 1: the MAC write data is ready and write to MAC table, self_clear	
1	RO	wtMAC_done	MAC write done → 1: MAC address write complete, read_clear	
2	RW	wtfilter	write filter bit	
5:3	RW	wtVLAN	Write VLAN number	
6	RW	wtVLAN_en	Write VLAN enable	
12:7	RW	wtP_number	write Port map number	
15:13	RW	wtage_field	Age-field → 000 empty 001 to 110 existed MAC 111 static address	
31:16	RW	wtMAC0	MAC write address [15:0]	

4.4.24 MAC_wt1, offset 0x5c

Bits	Type	Name	Description	Initial value
31:0	RW	wtMAC1	MAC write address [47:16]	

4.4.25 BW_cntl0, offset 0x60

Bits	Type	Name	Description	Initial value
2:0	RW	P0tx_bwcntl	Port0 transmit bandwidth control → 000: disable, 001: 111: 64K/128K/256K/512K/1M/4M/10M BIT PER Second	000
3		Reserved	Not Applicable	
6:4	RW	P0rx_bwcntl	Port0 receive bandwidth control	
7		Reserved	Not Applicable	
10:8	RW	P1tx_bwcntl	Port1 transmit bandwidth control	
11		Reserved	Not Applicable	
14:12	RW	P1rx_bwcntl	Port1 receive bandwidth control	
15		Reserved	Not Applicable	
18:16	RW	P2tx_bwcntl	Port2 transmit bandwidth control	
19		Reserved	Not Applicable	
22:20	RW	P2rx_bwcntl	Port2 receive bandwidth control	
23		Reserved	Not Applicable	
26:24	RW	P3tx_bwcntl	Port3 transmit bandwidth control	
27		Reserved	Not Applicable	
30:28	RW	P3rx_bwcntl	Port3 receive bandwidth control	
31		Reserved	Not Applicable	

4.4.26 BW_cntl1, offset 0x64

Bits	Type	Name	Description	Initial value
2:0	RW	P4tx_bwcntl	Port4 transmit bandwidth contro	
3		Reserved	Not Applicable	
6:4	RW	P4rx_bwcntl	Port4 receive bandwidth control	
7		Reserved	Not Applicable	
10:8	RW	P5tx_bwcntl	Port5 transmit bandwidth control	
11		Reserved	Not Applicable	
14:12	RW	P5rx_bwcntl	Port5 receive bandwidth control	
30:15		Reserved	Not Applicable	
31	RW	traffic shaper mode	The Transmit traffic shaper mode 1: average Inter Packet Gap (IPG) in the 1 second period (patent pending) 0: best effort mode (default)	0

4.4.27 PHY_cntl0, offset 0x68

Bits	Type	Name	Description	Initial value
4:0	RW	PHY_addr	PHY address	
7:5		Reserved	Not Applicable	
12:8	RW	PHY_register	PHY register address	
13	RW	WT_cmd	Write command, self_clear	

14	RW	RD_cmd	Read command, self_clear	
15		Reserved	Not Applicable	
31:16	RW	WT_data	The data be written into the PHY	

4.4.28 PHY_cntl1, offset 0x6c

Bits	Type	Name	Description	Initial value
0	RO	WT_done	Write operation is done, read_clear	
1	RO	RD_rdy	Read operation is complete and data is ready, read_clear	
15:2		Reserved	Not Applicable	
31:16	RO	RD_data	The read data	

4.4.29 FC_th, offset 0x70

Bits	Type	Name	Description	Initial value
7:0	RW	Drop2_set	Switch drop2 set threshold → 106 free blocks	
15:8	RW	Drop2_rls	Switch drop2 release threshold → 134 free blocks	
24:16	RW	FC_set	Switch flow control set threshold → 220 free blocks	
31:25		Reserved	Not Applicable	

Note: The working global thresholds = (register value) * 2, The Drop1_set[7:0] threshold default value = 137 blocks, The default working Drop1_set threshold = 137 x 2 =274.

4.4.30 adj_port_th, offset 0x74

Bits	Type	Name	Description	Initial value
3:0	RW	adj_port_th_H	per_port guaranteed normal priority pkt → 3 blocks	
7:4	RW	adj_port_th_L	per_port guaranteed high priority pkt → 3 blocks	
15:8		Reserved	Not Applicable	
24:16	RW	FC_rls	Switch flow control release threshold → 268 free blocks	
31:25		Reserved	Not Applicable	

4.4.31 Port_th, offset 0x78

Bits	Type	Name	Description	Initial value
7:0	RW	per_port_th	per port buffer threshold → 13 occupied blocks	
15:8	RW	CPU_th	CPU port buffer threshold → 48 occupied blocks	
23:16	RW	CPU_hold_th	the CPU hold threshold for all ports → default 120 free block	
31:24	RW	CPU_rls_th	the CPU hold release threshold → default 132 free block	

Note: Suggestion value is 0xE8DC1818h.

4.4.32 PHY_cntl2, offset 0x7c

Bits	Type	Name	Description	Initial value
4:0	RW	Auto-negotiation	Auto-negotiation enable. 1: Enable	
9:5	RW	Speed	Speed control. 1: 100M 0: 10M	
14:10	RW	Duplex	Duplex control. 1: Full 0: Half	

19:15	RW	fc_rec	the recommended FC value (reg4, bit10) → 0: no forced, 1: FC_rec ON	
24:20	RW	PHY reset	(default)	
29:25	RW	Auto MDIX	Per port PHY reset. 0: Reset. 1: Normal	
30	RW	Rec_mcc_average	Per port PHY auto MDIX enable Recommend MCC average enable Default value 0	
31		Reserved	Not Applicable	

4.4.33 PHY_cntl3, offset 0x80

Bits	Type	Name	Description	Initial value
1:0	RW	Rec_bslimit	Recommend base-line limit.	11
3:2	RW	FILTSEL	Pre-filter Recommend value.	10
5:4	RW	ISHSEL	Recommend Sample-Hold current.	00
6	RW	IINSEL	Default: 0	0
7	RW	APOLDIS	Recommend Auto Polarity disable.	0
8	RW	ENRJAB	Recommend receive jabber enable.	1
9	RW	DISJAB	Recommend transmit jabber disable.	0
10	RW	NTH	Recommend Normal threshold.	0
11	RW	FGDLINK	Recommend force good link.	0
13:12	RW	LFAILTM	Recommend polarity link fail timer select. Default: 00(2sec). (3,4,8 sec)???	00
14	RW	INTCHKEN	Recommend polarity LIU/LID interval check.	1
15	RW	CBDETEN	Recommend cable broken detect enable.	0
16	RW	DISFEFI	Disable far_end fault indication	
21:17	RW	FX_enable	Per port FX enable, default 0: disable	00000
31:22		Reserved	Not Applicable	

4.4.34 Pri_cntl, offset 0x84

Bits	Type	Name	Description	Initial value
5:0	RW	Port_pri	Force all the packet from the programmed port(s) are priority → 0: normal	
7:6		Reserved	Not Applicable	
13:8	RW	OffFC_en	Auto-turn-off FC when the programmed ports receive priority packet → 0: disable	
15:14		Reserved	Not Applicable	
19:16	RW	HN_rnd	The proportion of normal and high priority packet → 0000 - unlimited, 0001 - 8:1, 0010 – 16:1 …etc	
31:20		Reserved	Not Applicable	

4.4.35 VLAN_pri, offset 0x88

Bits	Type	Name	Description	Initial value
5:0	RW	VLAN_pri_en	Enable VLAN priority check → 0: disable ***Note***: [0] = port0, [1] = port 1 etc…	

7:6		Reserved	Not Applicable	
10:8	RW	VLAN_th	VLAN high priority threshold → if the priority field of VLAN tag ≧ this threshold, then the packet is high priority, default = 100	100
31:11		Reserved	Not Applicable	

4.4.36 TOS_en, offset 0x8c

Bits	Type	Name	Description	Initial value
5:0	RW	TOS_pri	Enable TCP/IP TOS priority check → 0: disable	
31:6		Reserved	Not Applicable	

4.4.37 TOS_map0, offset 0x90

Bits	Type	Name	Description	Initial value
31:0	RW	TOS_map0	TOS_bit_map[31:0]	

4.4.38 TOS_map1, offset 0x94

Bits	Type	Name	Description	Initial value
31:0	RW	TOS_map1	TOS_bit_map[64:32]	

4.4.39 Custom_pri1, offset 0x98

Bits	Type	Name		Initial value
11:0	RW	Custom_en	Enable custom packet check: 00: disable, default 01: treat as high priority 10: filtered, 11:reserved [1:0] = port0, [3:2] for port1 The packet type check → default = 0	
15:12		Reserved	Not Applicable	
31:16	RW	Custom_type	00: disable, default 01: treat as high priority 10: filtered, 11:reserved	

4.4.40 Custom_pri2, offset 0x9c

Bits	Type	Name	Description	Initial value
7:0	RW	Custom_define	Custom field define: default = 0	
15:8	RW	Custom_mask	The mask of custom field: default = 0	
23:16	RW	Offset	[7:0] offset count from SA: default = 0	

			If VLAN type found, it will add 4-byte automatically	
31:24		Reserved	Not Applicable	

4.4.41 PHY_cntl4, offset 0xA0

Bits	Type	Name	Description	
1:0	RO	P0_cbbrk_length	Port 0 cable broken length	
2	RO	P0_cbbrk	Port 0 cable broken	
3		Reserved	Not Applicable	
5:4	RO	P1_cbbrk_length	Port 1 cable broken length	
6	RO	P1_cbbrk	Port 1 cable broken	
7		Reserved	Not Applicable	
9:8	RO	P2_cbbrk_length	Port 2 cable broken length	
10	RO	P2_cbbrk	Port 2 cable broken	
11		Reserved	Not Applicable	
13:12	RO	P3_cbbrk_length	Port 3 cable broken length	
14	RO	P3_cbbrk	Port 3 cable broken	
15		Reserved	Not Applicable	
17:16	RO	P4_cbbrk_length	Port 4 cable broken length	
18	RO	P4_cbbrk	Port 4 cable broken	
19		Reserved	Not Applicable	
20	RW	volt23	1: 10BaseT voltage 2.3V, 0: 2.2V (default)	0
21	RW	rom_code25	1: fix the ROM code to 2.5V, 0: 2.2V (default)	0
31:22		Reserved	Not Applicable	

4.4.42 Empty_cnt, offset 0xA4

Bits	Type	Name	Description	Initial value
8:0	RO	empty_cnt	The empty block in the global buffer	
15:9		Reserved	Not Applicable	
22:16	RO	buffer_full_high	The high-pri out-queue full ports	
23		Reserved	Not Applicable	
30:24	RO	buffer_full_low	The low-pri out-queue full ports	
31		Reserved	Not Applicable	

4.4.43 Port_cnt_sel, offset 0xA8

Bits	Type	Name	Description	Initial value
3:0	RW	port_sel	The port selected for the port_cnt	
31:4		Reserved	Not Applicable	

4.4.44 Port_cnt, offset 0xAc

Bits	Type	Name		Initial value

	RO	sel_info	If port_sel=0, [24:16] port0 high packet count [8:0] port0 low packet count If port_sel=1, [24:16] port1 high packet count [8:0] port1 low packet count If port_sel=2, [24:16] port2 high packet count [8:0] port2 low packet count If port_sel=3, [24:16] port3 high packet count [8:0] port3 low packet count If port_sel=4, [24:16] port4 high packet count [8:0] port4 low packet count If port_sel=5, [24:16] port5 high packet count [8:0] port5 low packet count If port_sel=6, [24:16] port6 high packet count [8:0] port6 low packet count If port_sel=7, [24:16] port7 high packet count [8:0] port7 low packet count If port_sel=9, [8:0] flow control status If port_sel=10, [24:16] testing [8:0] ever flow control port If port_sel=11, [24:16] no_pkt status [7:0] no_pkt_status If port_sel=12, [24:16] receive bandwidth control port , [8:0] transmit bandwidth control port	

4.4.45 Int_st, offset 0xB0

Note: All bits are "write 1 clear"

Bits	Type		Description	Initial value
0	RW	send_H_done	DMA send one high priority packet to switch	
1	RW	send_L_done	DMA send one normal priority packet to switch	
2	RW	rx_H_done	DMA receive one high priority packet to CPU	
3	RW	rx_L_done	DMA receive one normal priority packet to CPU	
4	RW	H_Descriptor_full	The descriptor, "high priority receive", are full	
5	RW	L_Descriptor_ful	the descriptor, "normal priority receive", are full	
6	RW	port0_que_full	meet the port0 port-th & global empty-th	
7	RW	port1_que_full	meet the port1 port-th & global empty-th	
8	RW	port2_que_full	meet the port2 port-th & global empty-th	
9	RW	port3_que_full	meet the port3 port-th & global empty-th	
10	RW	port4_que_full	meet the port4 port-th & global empty-th	
11	RW	port5_que_full	meet the port5 port-th & global empty-th	
12		Reserved	Not Applicable	
13	RW	CPU_que_full	CPU port – meet the CPU port pre-th & global empty-th	
14	RW	Global_que_full	global empty-th	
15	RW	Must_drop	all the buffer almost full	

16	RW	BC_storm	accumulated BC count over BC_storm setting	
17		Reserved	Not Applicable	
18	RW	Port_status_chg	any port change the link status (link-up to/from link-down)	
19	RW	Intruder	any secured port has intruder packets	
20	RW	Watchdog0_tmr_expired	watchdog0 timer expired	
21	RW	Watchdog1_tmr_expired	Watchdog1 timer expired	
22	RW	rx_desc_err	receive descriptor error	
23	RW	send_desc_err	send descriptor error	
24	RW	CPU_hold	the CPU send packets are hold in descriptor	
31:25		Reserved	Not Applicable	

4.4.46 Int_mask, offset 0xB4

Note: 1: mask the interrupt

Bits	Type	Name	Description	Initial value
0	RW	M_send_H_done		
1	RW	M_send_L_done		
2	RW	M_rx_H_done		
3	RW	M_rx_L_done		
4	RW	M_H_Descriptor_full		
5	RW	M_L_Descriptor_full		
6	RW	M_port0_que_full		
7	RW	M_port1_que_full		
8	RW	M_port2_que_full		
9	RW	M_port3_que_full		
10	RW	M_port4_que_full		
11	RW	M_port5_que_full		
12		Reserved	Not Applicable	
13	RW	M_CPU_que_full		
14	RW	M_Global_que_full		
15	RW	M_Must_drop		
16	RW	M_BC_storm		
17		Reserved	Not Applicable	
18	RW	M_Port_status_chg		
19	RW	M_Intruder		
20	RW	M_Watchdog0_tmr_expired		
21	RW	M_Watchdog1_tmr_expired		
22	RW	M_rx_desc_err		
23	RW	M_send_desc_err		
24	RW	M_CPU_hold		
31:25		Reserved	Not Applicable	

4.4.47 GPIO_conf0, offset 0xB8

Bits	Type		Description	Initial value
7:0	RW	in_out0	GPIO[7:0] input or output → 1: input	
15:8	RO	in_value0	GPIO[7:0] input value if in the input mode	
23:16	RW	out_en0	GPIO[7:0] output enable if in the output mode → 0: input (default)	
31:24	RW	out_value0	GPIO[7:0] output value if in the output mode and enable	

4.4.48 GPIO_conf2, offset 0xBc

Bits	Type	Name	Description	Initial value
3:0		Reserved	Not Applicable	
4	WO	en_csx_intx	1: enable wait control, GPIO[0], for the CSX interface 0: disable	
5	WO	en_csx1_intx1	Enable CSX1, INTX1 in GPIO[3:4] → 0: disable	
6	WO	en_wait	Enable CSX, INTX in GPIO[1:2] → 0: disable	
31:7		Reserved	Not Applicable	

4.4.49 Watchdog0, offset 0xC0

Bits	Type	Name	Description	Initial value
14:0	RW	Watchdog0_tmr	Watchdog timer: count up timer, mask-able, write clear, unit 10ms. If reach timer set mean time up and keep the counter until write-clear by software, maximum 327sec.	
15		Reserved	Not Applicable	
30:16	RW	Watchdog0_tmr_set	Watchdog timer set: the time out setting of timer, if timer set is equal to timer, then it mean timer is expired. Maximum 32767	
31	RW	Watchdog0_reset_en	Watchdog timer trigger reset: 0: disable, 1: reset the whole chip, if watchdog timer expired	

4.4.50 Watchdog1, offset 0xC4

Bits	Type	Name	Description	Initial value
14:0	RW	Watchdog1_tmr	Watchdog1 timer: Count up timer, mask-able, write clear, unit 10ms. If reach timer set mean time up and keep the counter until write-clear by software, maximum 327sec.	
15		Reserved	Not Applicable	

30:16	RW	Watchdog1_tmr_set	Watchdog1 timer set: the time out setting of timer, if timer set is equal to timer, then it mean timer is expired. Maximum 32767	
31	RW	Watchdog1_drop_en	Watchdog timer stop CPU port receiving: 0: disable, 1: force all to CPU packets drop if timer is expired, and no issue flow control in ports. Auto-recover when the timer is cleaned	0

4.4.51 Swap_in, offset 0xC8

Bits	Type	Name	Description	Initial value
7:0	RW	Swap_din	Swap_din[7:0] = Swap_dout[31:24]	
15:8	RW	Swap_din	Swap_din[15:8] = Swap_dout[15:8]	
23:16	RW	Swap_din	Swap_din[23:16] = Swap_dout[15:8]	
31:24	RW	Swap_din	Swap_din[31:24] = Swap_dout[7:0]	

4.4.52 Swap_out, offset 0xCc

Bits	Type	Name	Description	Initial value
7:0	RO	Swap_dout	Swap_dout[7:0] = Swap_din[31:24]	
15:8	RO	Swap_dout	Swap_dout[15:8] = Swap_din[23:16]	
23:16	RO	Swap_dout	Swap_dout[23:16] = Swap_din[15:8]	
31:24	RO	Swap_dout	Swap_dout[31:24] = Swap_din[7:0]	

4.4.53 send_Hbaddr, offset 0xD0

Bits	Type	Name	Description	
24:0	RW	send_Hbaddr	The descriptor base address of CPU_to_SW (high priority)	
31:25		Reserved	Not Applicable	

Note: the loading base addresses need all four address registers been written. (i.e. send_Hbaddr, send_Lbaddar, receive_Hbaddar, and receive_Lbaddar)

4.4.54 send_Lbaddr, offset 0xD4

Bits	Type	Name	Description	Initial value
24:0	RW	send_LBaddr	The descriptor base address of CPU_to_SW (normal priority)	
31:25		Reserved	Not Applicable	

4.4.55 receive_Hbaddr, offset 0xD8

Bits	Type		Description	Initial value
24:0	RW	receive_HBaddr	The descriptor base address of SW_to_CPU (high priority)	

31:25		Reserved	Not Applicable	

4.4.56 receive_Lbaddr, offset 0xDc

Bits	Type	Name	Description	Initial value
24:0	RW	receive_LBaddr	The descriptor base address of SW_to_CPU (normal priority)	
31:25		Reserved	Not Applicable	

4.4.57 send_Hwaddr, offset 0xE0

Bits	Type	Name	Description	Initial value
24:0	RO	send_HWaddr	The descriptor WORKING address of CPU_to_SW (high priority)	
31:25		Reserved	Not Applicable	

4.4.58 send_Lwaddr, offset 0xE4

Bits	Type	Name	Description	Initial value
24:0	RO	port_sel	The descriptor WORKING address of CPU_to_SW (normal priority)	
31:25		Reserved	Not Applicable	

4.4.59 receive_Hwaddr, offset 0xE8

Bits	Type	Name	Description	Initial value
24:0	RO	receive_HWaddr	The descriptor WORKING address of SW_to_CPU (high priority)	
31:25		Reserved	Not Applicable	

4.4.60 receive_Lwaddr, offset 0xEc

Bits	Type	Name	Description	Initial value
24:0	RO	receive_LWaddr	The descriptor WORKING address of SW_to_CPU (normal priority)	
31:25		Reserved	Not Applicable	

4.4.61 Timer_int, offset 0xF0

Bits	Type	Name		Initial value
0	RW	time_out sataus	Write 1 clear	1
15:1		Reserved	Not Applicable	
16	RW	time_out_mask	1: mask the interrupt	1
31:17		Reserved	Not Applicable	

4.4.62 Timer, offset 0xF4

Bits	Type	Name		Initial value
15:0	RW	timer	unit 640ns, auto-reload, default 0xFFFF	
16	RW	timer_en	timer enable, 0: disable	0
31:17		Reserved	Not Applicable	

4.4.63 Reserved, offset 0xF8

Bits	Type	Name	Description	Initial value
31:0		Reserved	Not Applicable	

4.4.64 Reserved, offset 0xFc

Bits	Type		Description	Initial value
31:0		Reserved	Not Applicable	

4.4.65 port0_LED, offset 0x100

Bits	Type	Name	Description	Initial value
3:0	RW	p0_LED0	port0 LED[0] state, default = 1001, link/activity	1001
7:4	RW	p0_LED1	port0 LED[1] state, default = 0101, speed	0101
11:8	RW	p0_LED2	port0 LED[2] state, default = 1010, duplex/col	1010
14:12	RO	GPIOL_in[2:0]	the input value when programmed in input mode	
31:15		Reserved	Not Applicable	

Note: port0 LED[2:0] pin (164,165,166) configuration register

4.4.66 port1_LED, offset 0x104

Bits	Type	Name	Description	Initial value
3:0	RW	p1_LED0	port1 LED[0] state, default = 1001, link/activity	1001
7:4	RW	p1_LED1	port1 LED[1] state, default = 0101, speed	0101
11:8	RW	p1_LED2	port1 LED[2] state, default = 1010, duplex/col	1010
14:12	RO	GPIOL_in[5:3]	the input value when programmed in input mode	
31:15		Reserved	Not Applicable	

Note: port1 LED[2:0] pin (161,162,163) configuration register

4.4.67 port2_LED, offset 0x108

Bits	Type	Name	Description	Initial value
3:0	RW	p2_LED0	port2 LED[0] state, default = 1001, link/activity	1001
7:4	RW	p2_LED1	port2 LED[1] state, default = 0101, speed	0101
11:8	RW	p2_LED2	port2 LED[2] state, default = 1010, duplex/col	1010
14:12	RO	GPIOL_in[8:6]	the input value when programmed in input mode	

31:15		Reserved	Not Applicable	

Note: port2 LED[2:0] pin (147,158,160) configuration register

4.4.68 port3_LED, offset 0x10c

Bits	Type	Name	Description	Initial value
3:0	RW	P3_LED0	port3 LED[0] state, default = 1001, link/activity	1001
7:4	RW	P3_LED1	port3 LED[1] state, default = 0101, speed	0101
11:8	RW	P3_LED2	port3 LED[2] state, default = 1010, duplex/col	1010
14:12	RO	GPIOL_in[11:9]	the input value when programmed in input mode	
31:15		Reserved	Not Applicable	

Note: port3 LED[2:0] pin (144,145,146) configuration register

4.4.69 port4_LED, offset 0x110

Bits	Type	Name		Initial value
3:0	RW	p4_LED0	port4 LED[0] state, default = 1001, link/activity	1001
7:4	RW	p4_LED1	port4 LED[1] state, default = 0101, speed	0101
11:8	RW	p4_LED2	port4 LED[2] state, default = 1010, duplex/col	1010
14:12	RO	GPIOL_in[14:12]	the input value when programmed in input mode	
31:15		Reserved	Not Applicable	

Note: port4 LED[2:0] pin (141,142,143) configuration register

4.5 USB Control Status Register Map

Offset	Register	Offset	Register
0x00	General Control	0x40	Reserved
0x04	Interrupt Status	0x44	Reserved
0x08	Interrupt Enable	0x48	Reserved
0x0C	Reserved	0x4C	Reserved
0x10	Host General Control	0x50	Reserved
0x14	Reserved	0x54	Reserved
0x18	SOF Frame Number	0x58	Reserved
0x1C	SOF Frame Timer	0x5C	Reserved
0x20	Reserved	0x60	Reserved
0x24	Reserved	0x64	Reserved
0x28	Reserved	0x68	Reserved
0x2C	Reserved	0x6C	Reserved
0x30	Reserved	0x70	LS threshold
0x34	Reserved	0x74	RH DSCR
0x38	Reserved	0x78	PORT0 STS
0x3C	Reserved	0x7C	PORT1 STS
		0x80	Host descriptor head address

4.6 USB Control Status Registers Description

Host processors can only access USB 1.1 host/device controller registers with double word (32 bits) reads or writes on double word boundaries.

4.6.1 General Control , offset 0x00

Bits	Type	Name	Description	Initial value
0	R/W	HOST_EN	**USB Host function enable, Both modes:** This bit enables the USB host functions, when 1'b1, the controller acts as USB host	0
1	R/W	SW_INT_REQ	**Software interrupt request, Both modes:** When this bit is set to 1, the controller's interrupt pin become active. Reading this bit always returns zero. When SW_INT in interrupt is clear, this bit is clear as well.	0
2	R/W	DMA_ARB	**DMA Arbitration control, Both modes:** 0 : Receive = Transmit (1:1) 1 : Receive > Transmit	0
3	R/W	SW_RESET	**Software reset, Both modes:** Setting this bit resets the device controller to its initial state. This bit is auto-cleared after reset. Writing a 0 to this bit takes no effect.	0
31:4	RO	Reserved	Not Applicable	0

4.6.2 Interrupt Status, offset 0x04

Bits	Type	Name	Description	Initial value
3:0	R/W1C	Reserved	Not Applicable	0
4	R/W1C	SOF_INT	**SOF Transmitted/Received, Host mode:** 1: Issue a SOF token. The frame number value is stored in 0x1C Frame Number.	0
5	R/W1C	RES_INT	**Resume detected** 1: USB resume event is detected. Controller set this bit to one when resume signal is detected on USB bus.	0
6	R/W1C	Reserved	Not Applicable	0
7	R/W1C	Reserved	Not Applicable	0
8	R/W1C	BAB_INT	**Babble detected, Host mode:** 1: Detected babble.	0
9	R/W1	INSMOV_INT	**Root Hub status change:**	0

Bits	Type	Name	Description	Initial value
	C		1: Detected device insertion or remove. This bit will only be set for the device or hub, which is attached to host directly.	
10	R/W1C	SO	**Scheduling overrun** This bit is set when USB schedules for current frame overruns.	0
11	R/W1C	FNO	**Frame number overflow** This bit is set when the MSB of the frame number changes.	0
19:12	R/W1C	Reserved	Not Applicable	0
20	R/W1C	TD_Complete	**A TD is completed.**	0
25:21	R/W1C	Reserved	Not Applicable	0
28:26	RO	Reserved	Not Applicable	0
29	R/W1C	SW_INT	**Software interrupt, Both modes:** 1: Software Interrupt. This bit is set when software set one to SW_INT_REQ 0x00, and is cleared after software writes one to this bit.	0
30	R/W1C	FATAL_INT	**Fatal interrupt, Device mode:** Reserved. **Host mode:** 1:Fatal system bus error occurs.	0
31	RO	INT_ACT	**Interrupt active** When this bit is set, it indicates that at least one unmasked interrupt status is set.	0

4.6.3 Interrupt Enable, offset 0x08

Bits	Type	Name	Description	Initial value
30:0	R/W	INT_MASK	**Interrupt mask** Bits are set to allow the corresponding interrupts (bit 21:0 in Interrupt Status register) to generate an interrupt request. And cleared to prevent the interrupt from happening.	0
31	R/W	INT_EN	**Interrupt enable** 1: Enable the controller to assert interrupt, 0: Disable the controller to assert interrupt.	0

4.6.4 Reserved, offset 0x0C

Bits	Type	Name	Description	

31:0		Reserved	Not Applicable	

4.6.5 Host General Control, offset 0x10

Bits	Type	Name	Description	
1:0	R/W	BUS_STATE	**USB bus state** 00: USB reset state. 01: USB resume state. 10: USB operational state. 11: USB suspend state. A transition to USB operational state will cause the SOF generation to start 1 ms later.	2'b00
2	R/W	DMA_EN	**USB host DMA enable** This bit enables the host controller DMA functionality. When enable the DMA will start to fetch the descriptor for processing.	0
31:3	RO	Reserved	Not Applicable	0

4.6.6 Reserved, offset 0x14

Bits	Type	Name	Description	Initial value
31:0		Reserved	Not Applicable	

4.6.7 SOF Frame interval, offset 0x18

Bits	Type	Name	Description	Initial value
13:0	R/W	FM_INTERVAL	**Frame interval** This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. Software should store the current value of this field before resetting HC.	2EDFh
15:14	RO	Reserved	Not Applicable	0
30:16	R/W	FSLargestDataPacket	**FSLargestDataPacket** This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the software.	0
31	RO	FM_INTERVAL_TOG	**FrameIntervalToggle** Software toggles this bit whenever it loads a new value to FM_INTERVAL.	0

4.6.8 SOF Frame number, offset 0x1C

Bits	Type	Name	Description	Initial value
15:0	R/W	FM_NUM	**Frame number** This field is a 16-bit counter. It provides a timing reference among events happening in the Host Controller and the Host Controller Driver. The Host Controller Driver may use the 16-bit value specified in this register and generate a 32-bit frame number without requiring frequent access to the register.	0
29:16	R/W	FM_REMAININ G	**FrameRemaining** This counter is decremented at each bit time. When it reaches zero, it is reset by loading the frame Interval value specified in FM_INTERVAL at the next bit time boundary. When entering the USBOPERATIONAL state, HC re-loads the content with the FM_INTERVAL of and uses the updated value from the next SOF.	0
30	RO	Reserved	Not Applicable	0
31	R/W	FM_REMAININ G_TOG	**FrameRemaining toggle** This bit is loaded from the FM_INTERVAL_TOG field of FM_INTERVAL whenever FM_REMAIN remaining reaches 0. This bit is used by software for the synchronization between FM_INTERVAL and FM_REMAIN.	0

4.6.9 Reserved, offset 0x20 – 0x6C

Bits	Type	Name	Description	Initial value
31:0		Reserved	Not Applicable	

4.6.10 Low speed threshold, offset 0x70

Bits	Type	Name	Description	Initial value
11:0	R	LS_THRES	**Low Speed Threshold** This field contains a value which is compared to the FM_REMAIN field prior to initiating a Low Speed transaction. The transaction is started only if FM_REMAIN >= this field. The value is calculated by HCD with the consideration of transmission and setup overhead.	0628h
31:12	RO	Reserved	**Reserved**	0

4.6.11 RH descriptor, offset 0x74

Bits	Type	Name	Description	Initial value
7:0	RO	NUM_PORT		1
8	R/W	PSM	**Power Switch Mode** This bit is used to specify how the power switching of the Root Hub ports is controlled. It is implementation-specific. This field is only valid if the NPS field is cleared. 0: all ports are powered at the same time. 1: each port is powered individually. This mode allows portpower to be controlled by either the global switch or per-port switching. If the PPCM bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ClearGlobalPower).	0
9	R/W	NPS	**No Power Switch** These bits are used to specify whether power switching is supported or port are always powered. It is implementation-specific. When this bit is cleared, the PSM specifies global or per-port switching. 0: Ports are power switched 1: Ports are always powered on when the HC is powered on	0
10	R/W	OCPM	**OverCurrent protect Mode** This bit describes how the overcurrent status for the Root Hub ports are reported. At reset, this fields should reflect the same mode as PSM. This field is valid only if the NOCP field is cleared. 0: over-current status is reported collectively for alldownstream ports 1: over-current status is reported on a per-port basis	0
11	R/W	NOCP	**No OverCurrent protect** This bit describes how the overcurrent status for the Root Hub ports are reported. When this bit is cleared, the OCPM field specifies global or per-port reporting. 0: Over-current status is reported collectively for alldownstream ports 1: No overcurrent protection supported	0
15:12	RO	Reserved	Not Applicable	0
23:16	R/W	PPCM	Each bit indicates if a port is affected by a global power control command when PSM is set. When set, the port's power state is only affected by per-port power control (Set/ClearPortPower). When cleared, the port is controlled by the global power (switchSet/ClearGlobalPower). If the device	0

Bits	Type	Name	Description	Initial value
			is configured to global switching mode (PSM =0), this field is not valid. bit 0: Reserv ed bit 1: Ganged-power mask on Port #1 bit 2: Ganged-power mask on Port #2 ... bit7: Ganged-power mask on Port #7	
24	R/W	LPS	**Local power switch** (read) this bit is always read as ‘0’ . (write) ClearGlobalPower In global power mode (PSM =0), This bit is written to 1 to turn off power to all ports (clear PPS). In per-port power mode, it clears PPS only on ports whose PPCM bit is not set. Writing a 0 has no effect.	0
25	R/W	OCI	**Over current indication** This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If per-port overcurrent protection is implemented this bit is always 0	0
26	R/W	LPSC	**Local power switch change** (read) this bit is always read as 0. (write) SetGlobalPower In global power mode (PSM =0), This bit is written to 1 to turn on power to all ports (clear PPS). In per-port power mode, it sets PPS only on ports whose PPCM bit is not set. Writing a 0 has no effect.	0
27	R/W	OCIC	**Over current indication change** This bit is set by hardware when a change has occurred to the OCI field of this register. The HCD clears this bit by writing a 1. Writing a 0 has no effect.	0
28	R/W	DRWE	**Device remote wakeup enable** This bit enables a ConnectStatusChange bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the ResumeDetected interrupt. 0 = ConnectStatusChange is not a remote wakeup event. 1 = ConnectStatusChange is a remote wakeup event.	0
29	R/W	CRWE	**ClearRemoteWakeupEnable** Writing a '1' clears DeviceRemoveWakeupEnable . Writing a '0' has no effect.	0
31:30	RO	Reserved	Not Applicable	0

4.6.12 Port x status, offset 0x78

Bits	Type	Name	Description	
0	R/W	CCS	**Current connect status** (read)This bit reflects the current state of the downstream port. 0 = no device connected 1 = device connected (write)**ClearPortEnable** The HCD writes a 1 to this bit to clear the PES. Writing a 0 has no effect. The CCS is not affected by any write. Note: This bit is always read 1 when the attached device is nonremovable	0
1	R/W	PES	(read) **PortEnableStatus** This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PESC to be set. HCD sets this bit by writing SPE and clears it by writing CPE. This bit cannot be set when CCS is cleared. This bit is also set, if not already, at the completion of a port reset when RSC is set or port suspend when SSC is set. 0 = port is disabled 1 = port is enabled (write) **SetPortEnable** The HCD sets PortEnableStatus by writing a 1. Writing a 0 has no effect. If CCS is cleared, this write does not set PES, but instead sets CSC. This informs the driver that it attempted to enable a disconnected port.	0
2	R/W	PSS	(read)**PortSuspendStatus** This bit indicates the port is suspended or in the resume sequence. It is set by a SSS write and cleared when PSSC is set at the end of the resume interval. This bit cannot be set if CCS is cleared. This bit is also cleared when PRSC is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC. 0 = port is not suspended 1 = port is suspended (write) **SetPortSuspend** The HCD sets the PSS bit by writing a 1 to this bit. Writing a 0 has no effect. If CCS is cleared,	0

Bits	Type	Name	Description	Initial value
			this write does not set PSS; instead it sets CSC. This informs the driver that it attempted to suspend a disconnected port.	
3	R/W	POCI	(read) **PortOverCurrentIndicator** This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal 0 = no overcurrent condition. 1 = overcurrent condition detected. (write) **ClearSuspendStatus** The HCD writes a 1 to initiate a resume. Writing a 0 has no effect. A resume is initiated only if PSS is set.	0
4	R/W	PRS	(read) **PortResetStatus** When this bit is set by a write to SPR, port reset signaling is asserted. When reset is completed, this bit is cleared when PRSC is set. This bit cannot be set if CCS is cleared. 0 = port reset signal is not active 1 = port reset signal is active (write) **SetPortReset** The HCD sets the port reset signaling by writing a 1 to this bit Writing a 0 has no effect. If CCS is cleared, this write does not set PRS, but instead sets CSC. This informs the driver that it attempted to reset a disconnected port.	0
7:5	RO	Reserved	Not Applicable	0
8	R/W	PPS	(read) **PortPowerStatus** This bit reflects the port's power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing SPP or SGP. HCD clears this bit by writing CPP or CGP. Which power control switches are enabled is determined by PSM and PPCM[NDP] . In global switching mode (PSM =0), only Set/ClearGlobalPower controls this bit. In per-port power switching (PSM =1), if the PPCM[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CCS, PES, PSS, and PRS should be reset.	0

Bits	Type	Name	Description	Initial value
			0 = port power is off 1 = port power is on (write) **SetPortPower** The HCD writes a 1 to set the PPS bit. Writing a 0 has no effect. Note: This bit is always reads 1 if power switching is not supported.	
9	R/W	LSDV	(read) **LowSpeedDeviceAttached** This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set. 0 = full speed device attached 1 = low speed device attached (write) **ClearPortPower** The HCD clears the PortPowerStatus bit by writing a 1 to this bit. Writing a 0 has no effect.	0
15:10	RO	Reserved	Not Applicable	0
16	R/W	CSC	**ConnectStatusChange** This bit is set whenever a connect or disconnect event occurs. The HCD writes a 1 to clear this bit. Writing a 0 has no effect. If CCS is cleared when a SPR, SPE, or SPS write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected. 0 = no change in CCS 1 = change in CCS Note: this bit is set only after a Root Hub reset to inform the system that the device is attached.	0
17	R/W	PESC	**PortEnableStatusChange** This bit is set when hardware events cause the PES bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a 1 to clear this bit. Writing a 0 has no effect. 0 = no change in PES 1 = change in PES	0
18	R/W	PSSC	**PortSuspendStatusChange** This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resychronization delay. The HCD writes a 1 to clear this bit. Writing a 0 has no effect. This bit is also cleared when RSC is set. 0 = resume is not completed	0

Bits	Type	Name	Description	Initial value
			1 = resume completed	
19	R/W	OCIC	**OverCurrentIndicatorChange** This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the POCI bit. The HCD writes a 1 to clear this bit. Writing a 0 has no effect. 0 = no change in POCI 1 = OCI has changed	0
20	R/W	PRSC	**PortResetStatusChange** This bit is set at the end of the 10-ms port reset signal. The HCD writes a 1 to clear this bit. Writing a 0 has no effect. 0 = port reset is not complete 1 = port reset is complete	0
31:21	RO	Reserved	Not Applicable	0

4.6.13 Host Descriptor Head Starting Address, offset 0x80

Bits	Type	Name	Description	Initial value
3:0	RO	Reserved	Not Applicable	0
31:4	R/W	DSC_ADDR	**Descriptor Chain address** This field indicates the starting address of the host mode descriptor chain. DMA read the descriptor from this location when it is first enabled.	0

4.7 MPMC Registers

4.7.1 MPMC Registers Summary

Table 4-1 MPMC Registers Summary

Offset	Register
000h	MPMCControl
004h	MPMCStatus
008h	MPMCConfig
020h	MPMCDynamicControl
024h	MPMCDynamicRefresh
030h	MPMCDynamicRP
034h	MPMCDynamicRAS
038h	MPMCDynamicSREX
03Ch	MPMCDynamicAPR
040h	MPMCDynamicDAL

Offset	Register
044h	MPMCDynamicWR
048h	MPMCDynamicRC
04Ch	MPMCDynamicRFC
050h	MPMCDynamicXSR
054h	MPMCDynamicRRD
058h	MPMCDynamicMRD
080h	MPMCStaticExtendedWait
100h, 120h, 140h, 160h	MPMCDynamicConfig[0,1,2,3]
104h, 124h, 144h, 164h	MPMCDynamicRasCas[0,1,2,3]
200h, 220h, 240h, 260h	MPMCStaticConfig[0,1,2,3]
204h, 224h, 244h, 264h	MPMCStaticWaitWen[0,1,2,3]
208h, 228h, 248h, 268h	MPMCStaticWaitOen[0,1,2,3]
20Ch, 22Ch, 24Ch, 26Ch	MPMCStaticWaitRd[0,1,2,3]
210h, 230h, 250h, 270h	MPMCStaticWaitPage[0,1,2,3]
214h, 234h, 254h, 274h	MPMCStaticWaitWr[0,1,2,3]
218h, 238h, 258h, 278h	MPMCStaticWaitTurn[0,1,2,3]
FD0h	MPMCPeriphID4
FD4h, FD8h, FDCh	MPMCPeriphID5-7
FE0h	MPMCPeriphID0
FE4h	MPMCPeriphID1
FE8h	MPMCPeriphID2
FECh	MPMCPeriphID3

Offset	Register
FF0	MPMCPCellID0
FF4h	MPMCPCellID1
FF8h	MPMCPCellID2
FFCh	MPMCPCellID3

4.7.2 MPMC Control register, offset 000h

Bit #	Type	Name	Descriptions	Initial Value
0	R/W	E	MPMC Enable: indicates if the PrimeCell MPMC is enabled or disabled. 0 = disabled 1 = enabled (reset value on nPOR, and HRESETn). Disabling the PrimeCell MPMC reduces power consumption. When the memory controller is disabled the memory is not refreshed. The memory controller is enabled by setting the enable bit, or by system, or power-on reset.	1
1	R/W	M	Address mirror: indicates normal or reset memory map. 0 = normal memory map 1 = reset meory map. Static memory chip select 1 is mirrorred onto chip select 0 and chip select 4 (reset value on nPOR). On power-on reset, chip select 1 is mirrorred to both chip select 0 and chip select 1 and chip 4 memory areas. Clearing the M bit enables chip select 0 and chip select 4 memory to be accessed.	1
2	R/W	L	Low-power mode: indicate normal, or low-power mode. 0 = normal mode (reset value on nPOR, and HRESETn) 1 = low-power mode. Entering low-power mode reduces memory controller power consumption. Dynamic memory is refreshed as necessary. The memory controller returns to normal function mode by clearing the low-power mode bit (L), or by system, or power-on reset.	0
3	R/W	D	Drain write buffers: 0 = buffers operate normally (reset value on nPOR, and HRESETn) 1 = drain write buffers.	0
31:4		Reserved	Not Applicable	

4.7.3 MPMC Status register, offset 004h

Bit #	Type	Name	Descriptions	Initial Value
0	R	B	Busy: this read-only bit is used to ensure that the	0

Bit #	Type	Name	Descriptions	Initial Value
			memory controller enters the low-power or disabled mode cleanly: 0 = MPMC is idle (reset value on nPOR, and HRESETn) 1 = MPMC is busy performing memory transactions.	
1	R	S	Write buffer status: this read only bit enables the PrimeCell MPMC to enter low-power mode or disabled mode cleanly. 0 = write buffers empty (reset value on nPOR) 1 = write buffers contain data.	0
2	R	SREFACKA	Self-refresh acknowledge: this read only bit indicates the operating mode of the MPMC. 0 = normal mode (reset value on nPOR) 1 = self-refresh acknowledge.	0
31:3		Reserved	Not Applicable	

4.7.4 MPMC Config register, offset 008h

Bit #	Type	Name	Descriptions	Initial Value
0	R/W	N	Endian mode: 0 = little-endian mode 1 = big-endian mode. The value of the endian bit on power-on-reset (nPOR) is determined by the MPMCBIGENDIAN signal. This value can be overridden by software. This field is unaffected by the AHB reset (HRESETn).	0
8	R/W	CLK	Clock ratio: HCLK:MPMCCLKOUT[3:0] ratio. 0 = 1:1 (reset value on nPOR) 1 = 1:2.	0
7:1		Reserved	Read undefined, must be written as zeros.	
31:9		Reserved	Read undefined, must be written as zeros.	

4.7.5 MPMC Dynamic Control register, offset 020h

Bit #	Type	Name	Descriptions	Initial Value
0	R/W	CE	Dynamic memory clock enable: 0 = clock enable of devices are deasserted to save power (reset value on nPOR) 1 = all clock enables are driven HIGH continuously.	0
1	R/W	CS	Dynamic memory clock control: 0 = MPMCCLKOUT stops when all SDRAMs are idle and during self-refrsh mode 1 = MPMCCLKOUT runs continuously (reset value on nPOR). When clock control is LOW the output clock MPMCCLKOUT is stopped when there are no SDRAM transactions. The clock is also stopped during self-	1

Bit #	Type	Name	Descriptions	Initial Value
			refresh mode.	
2	R/W	MPMCSREFREQ (SR)	Self-refresh request: 0 = normal mode (reset value on nPOR) 1 = enter self-refresh mode. By writing 1 to this bit self-refresh can be entered under software control. Writing 0 to this bit returns the MPMC to normal mode. The self-refresh acknowledge bit in the MPMCStatus register must be polled to discover the current operating mode of the MPMC.	0
6:3		Reserved	Read undefined, must be written as zeros.	
8:7	R/W	I	SDRAM initialization: 00 = issue SDRAM NORMAL operation command (reset value on nPOR) 01 = issue SDRAM MODE command 10 = issue SDRAM PALL (precharge all) command 11 = issue SDRAM NOP (no operation) command.	00
12:9		Reserved	Read undefined, must be written as zeros.	
13	R/W	DP	Low-power SDRAM deep sleep mode: 0 = normal operation (reset value on nPOR) 1 = enter deep power down mode.	0
31:14		Reserved	Read undefined, must be written as zeros.	

4.7.6 MPMC Dynamic Refresh register, offset 024h

Bit #	Type	Name		Initial Value
10:0	R/W	REFRESH	Refresh timer: 0x0 = refresh disabled (reset value on nPOR) 0x1 1(x16) = 16 HCLK ticks between SDRAM refresh cycles 0x8 8(x16) = 128 HCLK ticks between SDRAM refresh cycles 0x1 to 0x7FF n(x16) = 16n HCLK ticks between SDRAM refresh cycles.	0x0
3:11		Reserved	Read undefined, must be written as zeros.	

4.7.7 MPMC Dynamic RP register, offset 030h

Bit #	Type	Name	Descriptions	Initial Value
3:0	R/W	tRP	Precharge command period: 0x0 to 0xE = n+1 clock cycle 0xF = 16 clock cycles (reset value on nPOR).	0xF
31:4		Reserved	Read undefined, must be written as zeros.	

Note:

The delay is in MPMCCLK cycles.

4.7.8 MPMC Dynamic RAS register, offset 034h

Bit #	Type	Name	Descriptions	Initial Value
3:0	R/W	tRAS	Active to precharge command period: 0x0 to 0xE = n+1 clock cycle 0xF = 16 clock cycles (reset value on nPOR).	0xF
31:4		Reserved	Read undefined, must be written as zeros.	

Note:
The delay is in MPMCCLK cycles.

4.7.9 MPMC Dynamic SREX register, offset 038h

Bit #	Type	Name	Descriptions	Initial Value
3:0	R/W	tSREX	Self-refresh exit time: 0x0 to 0xE = n+1 clock cycle 0xF = 16 clock cycles (reset value on nPOR).	0xF
31:4		Reserved	Read undefined, must be written as zeros.	

Note:
The delay is in MPMCCLK cycles.

4.7.10 MPMC Dynamic APR register, offset 03Ch

Bit #	Type	Name	Descriptions	Initial Value
3:0	R/W	tAPR	Last-data-out to active command time: 0x0 to 0xE = n+1 clock cycle 0xF = 16 clock cycles (reset value on nPOR).	0xF
31:4		Reserved	Read undefined, must be written as zeros.	

Note:
The delay is in MPMCCLK cycles.

4.7.11 MPMC Dynamic DAL register, offset 040h

Bit #	Type	Name	Descriptions	
3:0	R/W	tDAL	Data-in to active command time: 0x0 to 0xE = n+1 clock cycle 0xF = 16 clock cycles (reset value on nPOR).	0xF
31:4		Reserved	Read undefined, must be written as zeros.	

Note:
The delay is in MPMCCLK cycles.

4.7.12 MPMC Dynamic WR register, offset 044h

Bit #	Type	Name	Descriptions	Initial Value
3:0	R/W	tWR	Write recovery time: 0x0 to 0xE = n+1 clock cycle 0xF = 16 clock cycles (reset value on nPOR).	0xF
31:4		Reserved	Read undefined, must be written as zeros.	

Note:
The delay is in MPMCCLK cycles.

4.7.13 MPMC Dynamic RC register, offset 048h

Bit #	Type	Name	Descriptions	Initial Value
4:0	R/W	tRC	Active to active command period: 0x0 to 0x1E = n+1 clock cycle 0x1F = 32 clock cycles (reset value on nPOR).	0x1F
31:5		Reserved	Read undefined, must be written as zeros.	

Note:
The delay is in MPMCCLK cycles.

4.7.14 MPMC Dynamic RFC register, offset 04Ch

Bit #	Type	Name	Descriptions	Initial Value
4:0	R/W	tRFC	Auto refresh period and auto refresh to active command period: 0x0 to 0x1E = n+1 clock cycle 0x1F = 32 clock cycles (reset value on nPOR).	0x1F
31:5		Reserved	Read undefined, must be written as zeros.	

Note:
The delay is in MPMCCLK cycles.

4.7.15 MPMC Dynamic XSR register, offset 050h

Bit #	Type	Name	Descriptions	Initial Value
4:0	R/W	tXSR	Exit self-refresh to active command period: 0x0 to 0x1E = n+1 clock cycle 0x1F = 32 clock cycles (reset value on nPOR).	0x1F
31:5		Reserved	Read undefined, must be written as zeros.	

Note:
The delay is in MPMCCLK cycles.

4.7.16 MPMC Dynamic RRD register, offset 054h

Bit #	Type	Name	Descriptions	Initial Value
3:0	R/W	tRRD	Active bank A to active bank B latency: 0x0 to 0xE = n+1 clock cycle 0xF = 16 clock cycles (reset value on nPOR).	0xF
31:4		Reserved	Read undefined, must be written as zeros.	

Note:
The delay is in MPMCCLK cycles.

4.7.17 MPMC Dynamic MRD register, offset 058h

Bit #	Type	Name	Descriptions	Initial Value
3:0	R/W	tMRD	Load mode register to active command time: 0x0 to 0xE = n+1 clock cycle 0xF = 16 clock cycles (reset value on nPOR).	0xF

Bit #	Type	Name	Descriptions	Initial Value
31:4		Reserved	Read undefined, must be written as zeros.	

Note:
The delay is in MPMCCLK cycles.

4.7.18 MPMC Static Extended Wait register, offset 080h

Bit #	Type	Name	Descriptions	
9:0	R/W	EXTENDEDWAIT	External wait time out: 0x0 = n+1 clock cycle (reset value on nPOR) 0x1 to 0x3FF = (n+1)x16 clock cycles.	0x0
31:10		Reserved	Read undefined, must be written as zeros.	

Note:
The delay is in HCLK cycles.

4.7.19 MPMC Dynamic Config [0,1,2,3] register

Note: offset = 100h,120h, 140h, 160h respectively

Bit #	Type	Name	Descriptions	Initial Value
2:0		Reserved	Read undefined, must be written as zeros.	
4:3	R/W	MD	Memory device: 00=SDRAM(reset value on nPOR) 01=low-power SDRAM 10, 11=reserved.	00
6:5		Reserved	Read undefined, must be written as zeros.	
12:7	R/W	AM	Address mapping: See Table 3-5A 00000000=reset value on nPOR	00000000
13		Reserved	Read undefined, must be written as zeros.	
14	R/W	AM	Address mapping: See Table 3-5A 0=reset value on nPOR	0
18:15		Reserved	Read undefined, must be written as zeros.	
19	R/W	B	Buffer enable: 0=buffer disabled for accesses to this chip select(reset value on nPOR) 1=buffer enabled for accesses to this chip select.	0
20	R/W	P	Write protect: 0 = writes not protected (reset value on nPOR) 1 = write protected.	0
21		Reserved	Read undefined, must be written as zeros.	
24:22	R/W	CW	Column width: 000 = 6-bit (reset value on nPOR) 001 = 7-bit 010 = 8-bit 011 = 9-bit 100 = 10-bit	000

Bit #	Type	Name	Descriptions	Initial Value
			101 = 11-bit 110 = reserved 111 = reserved	
25		Reserved	Read undefined, must be written as zeros.	
26	R/W	NB	Number of banks: 0 = two banks (reset value on nPOR) 1 = four banks.	0
27		Reserved	Read undefined, must be written as zeros.	
29:28	R/W	RW	Row width: 00 = 11-bit (reset value on nPOR) 01 = 12-bit 10 = 13-bit 11 = reserved.	00
31:30		Reserved	Read undefined, must be written as zeros.	

Table 4-2 Address map

Address mapping				
[14]	**[12]**	**[11:9]**	**[8:7]**	**Description**
16-bit external bus High performance address mapping (Row, Bank, Column)				
0	0	000	00	16Mb (2Mx8), 2 banks, row length = 11, column length = 9
0	0	000	01	16Mb (1Mx16), 2 banks, row length = 11, column length = 8
0	0	001	00	64Mb (8Mx8), 4 banks, row length = 12, column length = 9
0	0	001	01	64Mb (4Mx16), 4 banks, row length = 12, column length = 8
0	0	010	00	128Mb (16Mx8), 4 banks, row length = 12, column length = 10
0	0	010	01	128Mb (8Mx16), 4 banks, row length = 12, column length = 9
0	0	011	00	256Mb (32Mx8), 4 banks, row length = 13, column length = 10
0	0	011	01	256Mb (16Mx16), 4 banks, row length = 13, column length = 9
0	0	100	00	512Mb (64Mx8), 4 banks, row length = 13, column length = 11
0	0	100	01	512Mb (32Mx16), 4 banks, row length = 13, column length = 10
16-bit external bus Low-power SDRAM address mapping (Bank, Row, Column)				
0	1	000	00	16Mb (2Mx8), 2 banks, row length = 11, column length = 9
0	1	000	01	16Mb (1Mx16), 2 banks, row length = 11, column length = 8
0	1	001	00	64Mb (8Mx8), 4 banks, row length = 12, column length = 9
0	1	001	01	64Mb (4Mx16), 4 banks, row length = 12, column length = 8
0	1	010	00	128Mb (16Mx8), 4 banks, row length = 12, column length = 10
0	1	010	01	128Mb (8Mx16), 4 banks, row length = 12, column length = 9
0	1	011	00	256Mb (32Mx8), 4 banks, row length = 13, column length = 10
0	1	011	01	256Mb (16Mx16), 4 banks, row length = 13, column length = 9
0	1	100	00	512Mb (64Mx8), 4 banks, row length = 13, column length = 11
0	1	100	01	512Mb (32Mx16), 4 banks, row length = 13, column length = 10

32-bit external bus High performance address mapping (Row, Bank, Column)				
1	0	000	00	16Mb (2Mx8), 2 banks, row length = 11, column length = 9
1	0	000	01	16Mb (1Mx16), 2 banks, row length = 11, column length = 8
1	0	001	00	64Mb (8Mx8), 4 banks, row length = 12, column length = 9
1	0	001	01	64Mb (4Mx16), 4 banks, row length = 12, column length = 8
1	0	001	10	64Mb (2Mx32), 4 banks, row length = 11, column length = 8
1	0	010	00	128Mb (16Mx8), 4 banks, row length = 12, column length = 10
1	0	010	01	128Mb (8Mx16), 4 banks, row length = 12, column length = 9
1	0	010	10	128Mb (4Mx32), 4 banks, row length = 12, column length = 8
1	0	011	00	256Mb (32Mx8), 4 banks, row length = 13, column length = 10
1	0	011	01	256Mb (16Mx16), 4 banks, row length = 13, column length = 9
1	0	011	10	256Mb (8Mx32), 4 banks, row length = 13, column length = 8
1	0	100	00	512Mb (64Mx8), 4 banks, row length = 13, column length = 11
1	0	100	01	512Mb (32Mx16), 4 banks, row length = 13, column length = 10
32-bit external bus Low-power SDRAM address mapping (Bank, Row, Column)				
1	1	000	00	16Mb (2Mx8), 2 banks, row length = 11, column length = 9
1	1	000	01	16Mb (1Mx16), 2 banks, row length = 11, column length = 8
1	1	001	00	64Mb (8Mx8), 4 banks, row length = 12, column length = 9
1	1	001	01	64Mb (4Mx16), 4 banks, row length = 12, column length = 8
1	1	001	10	64Mb (2Mx32), 4 banks, row length = 11, column length = 8
1	1	010	00	128Mb (16Mx8), 4 banks, row length = 12, column length = 10
1	1	010	01	128Mb (8Mx16), 4 banks, row length = 12, column length = 9
1	1	010	10	128Mb (4Mx32), 4 banks, row length = 12, column length = 8
1	1	011	00	256Mb (32Mx8), 4 banks, row length = 13, column length = 10
1	1	011	01	256Mb (16Mx16), 4 banks, row length = 13, column length = 9
1	1	011	10	256Mb (8Mx32), 4 banks, row length = 13, column length = 8
1	1	100	00	512Mb (64Mx8), 4 banks, row length = 13, column length = 11
1	1	100	01	512Mb (32Mx16), 4 banks, row length = 13, column length = 10

4.7.20 MPMC Dynamic Ras Cas[0,1,2,3] register

Note: offset = 200h, 220h, 240h is for SMC_CSZ0, SMC_CSZ1, and SMC_CSZ2 respectively

Bit #	Type	Name	Descriptions	
1:0	R/W	RAS	RAS latency (active to read or write delay): 00=reserved 01=one clock cycle(a) 10=two clock cycles 11=three clock cycles (reset value on nPOR).	11
7:2		Reserved	Read undefined, must be written as zeros.	
9:8	R/W	CAS	CAS latency: 00=reserved 01=one clock cycle(a) 10=two clock cycle 11=three clock cycle(reset value on nPOR).	11
31:10		Reserved	Read undefined, must be written as zeros.	

Note:
The RAS to CAS latency (RAS) and CAS latency (CAS) are both defined in MPMCCLK cycles.

4.7.21 MPMC Static Config[0,1,2,3] register

Note: offset = 200h, 220h is for F_CS1_N and F_CS0_N respectively.

Bit #	Type	Name	Descriptions	Initial Value
1:0	R/W	MW	Memory width: 00 = 8bit 01 = 16bit 10 = 32bit 11 = reserved. The value of the F_CS0_N controlled memory width field is determined by reset latched value of A[18:17]	00(default value for SMC_CSZ0, SMC_CSZ2, SMC_CSZ3)
2		Reserved	Read undefined, must be written as zeros.	
3	R/W	PM	Page mode: 0=disabled (reset value on nPOR) 1=async page mode four enabled.	0
5:4		Reserved	Read undefined, must be written as zeros.	
6	R/W	PC	Chip select polarity: 0 = active LOW chip select 1 = active HIGH chip select. The value of the chip select polarity on power-on-reset (nPOR) is determined by the relevant MPMCSxPOL signal. This value can be overridden by software. This field is Unaffected by AHB reset (HRESETn).	
7	R/W	PB	Byte lane state: 0 = For reads all the bits in nMPMCBLSOUT[3:0] are	0

Bit #	Type	Name	Descriptions	Initial Value
			HIGH (reset value on nPOR).For writes the respective active bits in nMPMCBLSOUT[3:0] are LOW. 1 = For reads the respective active bits in nMPMCBLSOUT[3:0] are LOW. For writes the respective active bits in nMPMCBLSOUT[3:0] are LOW.	
8	R/W	EW	Extended wait: 0 = extended wait disabled (reset value on nPOR) 1=extended wait enabled.	0
18:9		Reserved	Read undefined, must be written as zeros.	
19	R/W	B	Buffer enable: 0 = write buffer disabled (reset value on nPOR) 1=write buffer enabled.	0
20	R/W	P	Write protect: 0 = writes not protected (reset value on nPOR) 1 = write protected.	0
31:21		Reserved	Read undefined, must be written as zeros.	

Note:
Synchronous burst mode memory devices are not supported.

4.7.22 MPMC Static Wait Wen [0,1,2,3] register

Note: offset = 200h, 220h, 240h is for SMC_CSZ0, SMC_CSZ1, and SMC_CSZ2 respectively

Bit #	Type	Name	Descriptions	Initial Value
3:0	R/W	WAITWEN	Wait write enable: delay from chip select assertion to write enable. 0000 = one HCLK cycle delay between assertion of chip select and write enable (reset value on nPOR) 0001 to 1111 = (n+1) HCLK cycle delay.	0000
31:4		Reserved	Read undefined, must be written as zeros.	

Note:
The delay is (WAITWEN+1) x tHCLK.

4.7.23 MPMC Static Wait Oen[0,1,2,3] register

Note: offset = 200h, 220h, 240h is for SMC_CSZ0, SMC_CSZ1, and SMC_CSZ2 respectively

Bit #	Type		Descriptions	Initial Value
3:0	R/W	WAITOEN	Wait output enable: delay from chip select assertion to output enable. 0000 = No delay (reset value on nPOR) 0001 to 1111 = n cycle delay.	0000
31:4		Reserved	Read undefined, must be written as zeros.	

Note:
The delay is WAITOEN x tHCLK.

4.7.24 MPMC Static Wait Rd [0,1,2,3] register

Note: offset = 200h, 220h, 240h is for SMC_CSZ0, SMC_CSZ1, and SMC_CSZ2 respectively

Bit #	Type	Name	Descriptions	Initial Value
4:0	R/W	WAITRD	Nonpage mode read wait states or asynchronous page mode read first access wait state. Nonpage mode: 00000 to 11110 = (n+1) HCLK cycles for read accesses 11111 = 32 HCLK cycles for read accesses(reset value on nPOR). Asynchronous page mode read, first read only: 00000 to 11110 = (n+1) HCLK cycles for burst read accesses 11111 = 32 HCLK cycles for page read accesses (reset value on nPOR)	11111
31:5		Reserved	Read undefined, must be written as zeros.	

Note:
For non-sequential reads, the wait state time is (WAITRD+1) x tHCLK.

4.7.25 MPMC Static Wait Page [0,1,2,3] register

Note: offset = 200h, 220h, 240h is for SMC_CSZ0, SMC_CSZ1, and SMC_CSZ2 respectively

Bit #	Type	Name	Descriptions	Initial Value
4:0	R/W	WAITPAGE	Asynchronous page mode read after the first access wait states: number of wait states for asynchronous page mode read accesses after the first read. 00000 to 11110 = (n+1) HCLK cycle read access time 11111 = 32 HCLK cycle read access time (reset value on nPOR).	11111
31:5		Reserved	Read undefined, must be written as zeros.	

Note:
For asynchronous page mode read for sequential reade,the wait state time for page mode accesses after the first read is (WAITPAGE+1) x tHCLK.

4.7.26 MPMC Static Wait Wr [0,1,2,3] register

Note: offset = 200h, 220h, 240h is for SMC_CSZ0, SMC_CSZ1, and SMC_CSZ2 respectively

Bit #	Type	Name		Initial Value
4:0	R/W	WAITWR	Write wait states: SRAM wait state time for write accesses after the first read.	11111

Bit #	Type	Name	Descriptions	Initial Value
			00000 to 11110 = (n+2) HCLK cycle write access time 11111 = 33 HCLK cycle write access time (reset value on nPOR).	
31:5		Reserved	Read undefined, must be written as zeros.	

Note:
The wait state time for write accesses after the first read is WAITWR x tHCLK.

4.7.27 MPMC Static Wait Turn [0,1,2,3] register

Note: offset = 200h, 220h, 240h is for SMC_CSZ0, SMC_CSZ1, and SMC_CSZ2 respectively

Bit #	Type	Name	Descriptions	Initial Value
3:0	R/W	WAITTURN	Bus turnaround cycles: 0000 to 1110 = (n+1) HCLK turnaround cycles 1111 = 16 HCLK turnaround cycles (reset value on nPOR).	1111
31:4		Reserved	Read undefined, must be written as zeros.	

Note:
Bus turnaround time is (WAITTURN+1) x tHCLK.

4.7.28 Conceptual MPMC Additional Peripheral ID register

Bit #	Type	Name	Descriptions	Initial Value
7:0	R	Configuration1	Additional peripheral configuration information.	0
31:8	W	Reserved	Read undefined, must be written as zeros.	0

Note:
The configuration options are peripheral-specific. For MPMC, the four, eight-bit peripheral identification registers are described in the following sections:

4.7.29 MPMC PeriphID4 register, offset FD0h

Bit #	Type	Name	Descriptions	Initial Value
0	R	Configuration	Static memory interface: 0=no 1=yes (value for PL172).	1
2:1	R	Configuration	Number of read/write buffers: 00=4 buffers (value for PL172) 01=8 buffers 10=12 buffers 11=16 buffers..	00
31:3		Reserved	Read undefined, must be written as zeros.	

Note:
The MPMCPeriphID4 register is hard-coded and the fields within the register determine the reset value.

4.7.30 MPMC PeriphID5-7 register, offset FD4h, FD8h, FDCh

Bit #	Type	Name	Descriptions	Initial Value
31:0		Reserved	Read undefined, must be written as zeros.	0

4.7.31 Conceptual MPMC Peripheral ID register

Bit #	Type	Name	Descriptions	Initial Value
11:0	R	Part number	Identifies the peripheral. The part number for PL175 is 0x175.	175
19:12	R	Designer	Designer's ID number. This is 0x41 for ARM.	41
23:20	R	Revision	The peripheral revision number is revision dependent.	0
31:24	R	Configuration	Configuration options are peripheral-specific. See MPMCPeriphID3 register	0

Note:

The four eight-bit peripheral identification registers are described in the following sections:
MPMCPeriphID0 register
MPMCPeriphID1 registers on next page.
MPMCPeriphID2 registers on next page.
MPMCPeriphID3 registers on next page.

4.7.32 MPMC PeriphID0 register, offset FE0h

Bit #	Type	Name	Descriptions	Initial Value
7:0	R	PartNumber0	These bits read back as 0x72.	72
31:8		Reserved	Read undefined, must be written as zeros.	

Note:

The MPMCPeriphID0 register is hard-coded and the fields within the register determine the reset value.

4.7.33 MPMCPeriphID1 register, offset FE4h

Bit #	Type	Name		Initial Value
3:0	R	PartNumber1	These bits read back as 0x1.	1
7:4	R	Designer0	These bits read back as 0x1.	1
31:8		Reserved	Read undefined, must be written as zeros.	

Note:

The MPMCPeriphID1 register is hard-coded and the fields within the register determine the reset value.

4.7.34 MPMC PeriphID2 register, offset FE8h

Bit #	Type		Descriptions	Initial Value
3:0	R	Designer1	These bits read back as 0x4.	4
7:4	R	Revision	These bits read back as the revision number,which can be between 0 and 15.	0
31:8		Reserved	Read undefined, must be written as zeros.	

Note:

The MPMCPeriphID2 register is hard-coded and the fields within the register determine the reset value.

4.7.35 MPMC PeriphID3 register, offset FECh

Bit #	Type	Name	Descriptions	
2:0	R	Configuration	Indicates the number of AHB slave ports: 000=1 AHB slave port 001=2 AHB slave port 010=4 AHB slave port 011=6 AHB slave port 100=8 AHB slave port 101-111=reserved For PL172 this field is set to 010.	010
5:3	R	Configuration	Indicates the AHB master bus width: 000=32-bit wide 001=64-bit wide 010=128-bit wide 011=256-bit wide 100=512-bit wide 101=1024-bit wide 110-111=reserved For PL172 this field is set to 000.	0
6	R	Configuration	Data buffers: 0=no 1=yes For PL172 this field is set to 1.	1
7	R	Configuration	TIC interface: 0=no 1=yes For PL172 this field is set to 1.	1
31:8		Reserved	Read undefined, must be written as zeros.	

Note:

The MPMCPeriphID2 register is hard-coded and the fields within the register determine the reset value.

4.7.36 MPMC PrimeCellID register, offset 00h

Bit #	Type	Name		Initial Value
7:0	R		The reset value = 0x0D (held by MPMCPCellID0).	0D
15:8	R		The reset value = 0xF0 (held by MPMCPCellID1).	F0
23:16	R		The reset value = 0x05 (held by MPMCPCellID2).	05
31:24	R		The reset value = 0xB1 (held by MPMCPCellID3).	B1

4.7.37 MPMC PCellID0 register, offset FF0h

Bit #	Type	Name	Descriptions	
7:0	R		These bits read back as 0x0D.	0D
31:8		Reserved	Read undefined, must be written as zeros.	

4.7.38 MPMC PCellID1 register, offset FF4h

Bit #	Type		Descriptions	Initial Value
7:0	R		These bits read back as 0xF0.	F0
31:8		Reserved	Read undefined, must be written as zeros.	

4.7.39 MPMCPCellID2 register, offset FF8h

Bit #	Type		Descriptions	Initial Value
7:0	R		These bits read back as 0x05.	5
31:8		Reserved	Read undefined, must be written as zeros.	

4.7.40 MPMCPCellID3 register, offset FFCh

Bit #	Type	Name	Descriptions	Initial Value
7:0	R		These bits read back as 0xB1.	8'hB1
31:8		Reserved	Read undefined, must be written as zeros.	

4.8 UART Registers

4.8.1 Remap and Pause Controller Registers

Table 4-3 Remap and Pause Controller Registers Summary

Offset	Name	Descriptions
00h		UART data register
04h		UART receive status register/error clear register
08h	UARTLCR_H	UART line control register, high byte
0ch	UARTLCR_M	UART line control register, middle byte
10h	UARTLCR_L	UART line control register, low byte
14h	UARTCR	UART control register
18h	UARTFR	UART flag register
1ch	UARTIIR/UARTICR	UART interrupt identification register/interrupt clear register

4.8.2 UART data register, offset 00h

Bit #	Type	Name	Descriptions	Initial Value
7:0	R/W	UARTDR	Receive (read) data character Transmit (write) data character	0

4.8.3 UART receive status register/error clear register, offset 04h

Bit #	Type		Descriptions	Initial Value
0	R	FE	Framing Error (FE): When this bit is set to 1, it indicates that the received character did not have a valid stop bit.	0
1	R	PE	Parity Error (PE): When this bit is set to 1, it indicates that the parity of received data character does pot match the parity selected in UARTLCR_H (bit 2)	0
2	R	BE	Break Error (BE): This bit is set to 1 if a break condition was detected, indicating that the received data input was held LOW for longer than a full-word transmission time.	0
3	R	OE	Overrun Error (OE): This bit is set to 1 if data is received and the FIFO is already full.	0
6:4		Reserved	Not Applicable	
7	W	RSR	A write to this register clears the framing, parity, break and overrun errors. The data value is not important.	0

4.8.4 UART line control register, high byte, offset 08h

Bit #	Type	Name	Descriptions	Initial Value
0	R/W	BRK	Send Break: If this bit is set to 1, a low level is continually output on the UARTTXD output, after completing transmission of the current character. This bit must be asserted for at least one complete frame transmission time in order to generate a break condition. The transmit FIFO contents remain unaffected during a break condition. For normal use, this bit must be cleared to 0.	0
1	R/W	PEN	Parity enable: If this bit is set to 1, parity checking and generation is enabled, else parity is disabled and no parity bit assed to the data frame.	0
2	R/W	EPS	Even Parity Select: If this bit is set to 1, even parity generation and checking is performed during transmission and reception, which checks for an even number of 1s in data and parity bits. When cleared to 0 then odd parity is performed which checks for an odd number of 1s.this bit has no effect when parity is disabled by parity enable being cleared to 0.	0

Bit #	Type	Name	Descriptions	Initial Value
3	R/W	STP2	Two Stop Bits Select: If this bit is set to 1, two stop bits are transmitted at the end of the frame. The receive logic does not check for two stop bits being received.	0
4	R/W	FEN	Enable FIFOs: If this bit is set to 1,transmit and receive FIFO buffers are enabled (FIFO mode). When cleared to 0 the FIFOs are disable (character mode) that is, the FIFOs become 1 byte-deep holding register.	0
6:5	R/W	WLEN	Word length [1:0] The select bits indicate the number of data bits transmitted or received in a frame as follows: 11 = 8 bits 10 = 7 bits 01 = 6 bits 00 = 5 bits	00
7		Reserved	Not Applicable	

4.8.5 UART line control register, middle byte, offset 0ch

Bit #	Type	Name	Descriptions	Initial Value
7:0	R/W	BAUD DIVMS	Most significant byte of baud rate divisor. These bits are cleared to 0 on reset.	0

4.8.6 UART line control register, low byte, offset 10h

Bit #	Type	Name	Descriptions	Initial Value
7:0	R/W	BAUD DIVLS	Least significant byte of baud rate divisor. These bits are cleared to 0 on reset.	0

Note:

The baud rate divisor is calculated as follow:

Baud rat divisor BAUDDIV = (FUARTCLK/(16*Baud rate))-1

Where FUARTCLK is the UART reference clock frequency

The below table show some typical bit rates and their corresponding divisor, given a UART clock frequency of 62.5 MHz. A divisor value of zero is illegal, and so no transmission or reception will occur.

4.8.7 UART control register (UARTCR), offset 14h

Bit #	Type		Descriptions	Initial Value
0	R/W	UARTEN	UART enable: If this bit set to 1, the UART is enabled.	0
2:1		Reserved	Not Applicable	
3	R/W	MSIE	Modem status interrupt enable: If this bit is set to 1, the modem interrupt is enabled. The modem status interrupt is asserted if any of the modem status lines (CTS,DCD,DSR) change.	0

Bit #	Type	Name	Descriptions	Initial Value
			Modem status change when one of the following events occurs: (1) 0 → 1 (2) 1 → 0	
4	R/W	RIE	Receive interrupt enable: If this bit is set to 1, the receive interrupt is enabled. Thereceive interrupt changes state when one of the following events occurs: 1.if the FIFOs are enabled and the receive FIFO is half or more full, then the receive interrupt is asserted HIGH. It is cleared by reading data from the receive FIFO until it becomes less than half full. 2.if the FIFOs are disabled and data is received thereby filling the location, the receive interrupt is asserted HIGH. The receive interrupt is cleared by performing a single read to the receive FIFO.	0
5	R/W	TIE	Transmit interrupt enable: If this bit is set to 1, the transmit interrupt is enabled. The transmit interrupt changes state when one of the following events occurs: 1.if the FIFOs are enabled and the transmit FIFO is at least half empty, then the transmit interrupt is asserted HIGH. It is cleared by filling the transmit FIFO to more than half full. 2.if the FIFOs are disabled and there is no data preset in the transmitters single location, the transmit FIFO is asserted HIGH. It is cleared by performing a single write to the transmitter FIFO.	0
6	R/W	RTIE	Receive timeout interrupt enable: If this bit is set to 1, the receive timeout interrupt is enabled. The receive timeout interrupt is asserted when the receive FIFO is not empty and no further data is received over a 32-bit period. The receive timeout interrupt is cleared when the FIFO becomes empty through reading al the data.	0
7		Reserved	Not Applicable	

4.8.8 UART flag register (UARTFR), offset 18h

Bit #	Type	Name	Descriptions	Initial Value
0	RO	CTS	This bit is the complement of the UART clear to send (nUARTCTS) modem status input. That is , the bit is 1 when the modem status input is 0.	0
1	RO	DSR	This bit is the complement of the UART data set ready	0

Bit #	Type	Name	Descriptions	Initial Value
			(nUARTDSR) modem status input. That is , the bit is 1 when the modem status input is 0.	
2	RO	DCD	This bit is the complement of the UART data carrier detect (nUARTDCD) modem status input. That is , the bit is 1 when the modem status input is 0.	0
3	RO	BUSY	UART Busy: If this bit is set to 1, the UART is busy transmitting data. This bit remains set until the complete byte, including all the stop bits, has been sent from he shift register. This bit is set as soon as the transmit FIFO becomes non-empty.	0
4	RO	RXFE	Receive FIFO Empty: The meaning of this bit depends on the state of the FEN bit in the UARTLCR_H register. If the FIFO is disabled, this bits is set when receive holding register is empty. If the FIFO is enabled, the RXFE bit is set when the receive FIFO is empty.	1
5	RO	TXFF	Transmit FIFO Full: The meaning of this bit depends on the state of the FEN bit in the UARTLCR_H register. If the FIFO is disabled, this bit is set when transmit holding register is full. If the FIFO is enabled, the RXFE bit is set when the transmit FIFO is full.	0
6	RO	RXFF	Receive FIFO Full: The meaning of this bit depends on the state of the FEN bit in the UARTLCR_H register. If the FIFO is disabled, this bit is set when the receive holding register is full. If the FIFO is enabled, the RXFF bit is set when receive FIFO is full.	0
7	RO	TXFE	Transmit FIFO Empty: The meaning of this bit depends on the state of the FEN bit in the UARTLCR_H register If the FIFO is disabled, this bit is set when the transmit holding register is empty. If the FIFO is enabled, the TXFE bit is set when the transmit FIFO is empty.	1

4.8.9 UARTIIR/UARTICR, offset 1ch

Bit #	Type	Name	Descriptions	Initial Value
0	R	MIS	This bit is set to 1 if the UARTRTINTR modem status interrupt is asserted.	0
1	R	RIS	This bit is set to 1 if the UARTRTINTR receive interrupt is asserted.	0
2	R	TIS	This bit is set to 1 if the UARTRTINTR transmit interrupt is asserted.	0
3	R	RTIS	This bit is set to 1 if the UARTRTINTR receive timeout interrupt is asserted.	0
6:4		Reserved	Not Applicable	
7	W	UARTICR	A write to this register clears the modem status interrupt, regardless of the value written.	0

Chapter 5 Electrical Specification

5.1 Absolute Maximum Ratings

Supply Voltage (Vcc)	-0.5 V to 1.9 V
Input Voltage	-0.5 V to VCC + 0.3 V
Output Voltage	-0.5 V to VCC + 0.3 V
Storage Temperature	-65 °C to 150 °C(-85°F to 302°F)
Ambient Temperature	0°C to 70°C(32°F to 158°F)
ESD Protection	2000V

5.2 DC Specifications

Parameter	Description	Condition	Min	Typical	Max	Units
Vcc	Supply Voltage		1.7	1.8	1.9	V
Vcc	Supply Voltage (I / O)		3.0	3.3	3.6	V
Icc	Power Supply	Vcc = 1.8V				mA
Icc	Power Supply (I / O)	Vcc = 3.3V				mA
Vil	Input LOW Voltage		-0.5		0.8	V
Vih	Input HIGH Voltage		2.0		3.8	V
Iil	Input LOW Leakage Current	Vin = 0.8V	-10		10	uA
Iih	Input HIGH Leakage Current	Vin = 2.0V	-10		10	uA
Vol	Output LOW Voltage	Iout =2~8mA			0.4	V
Voh	Output HIGH Voltage	Iout =-2~-8mA	2.4			V
Cinp	Input Pin Capacitance		5		8	pF
Lpinp	Pin Inductance		N/A			nH

5.3 AC Timing

5.3.1 SDRAM interface

(Unit: ns, Min: best case, Max: worst case)

Signal Name	Description	Edge
Tck	clock cycle time	P
Tps	command/address setup delay time in precharge stage	P
Tph	command/address hold delay time in precharge stage	P
Tas	command/address setup delay time in active stage	P
Tah	command/address hold delay time in active stage	P
Tws	command/address setup delay time in write stage	P
Twh	command/address hold delay time in write stage	P
Trs	command/address setup delay time in read stage	P
Trh	command/address hold delay time in read stage	P

Note:
P means positive edge.

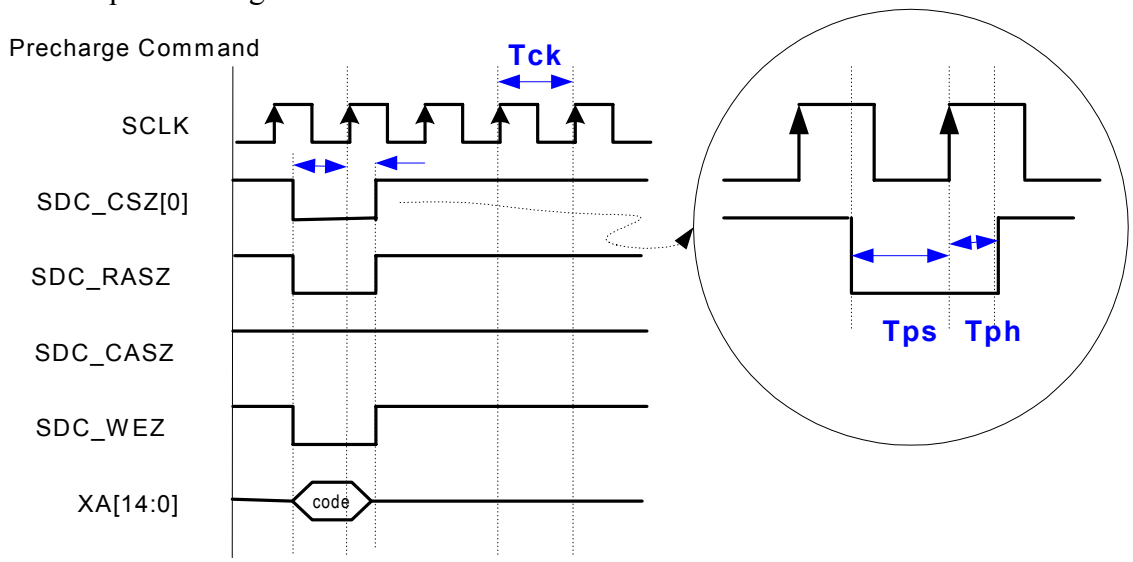


Figure 5-1 Precharge Command

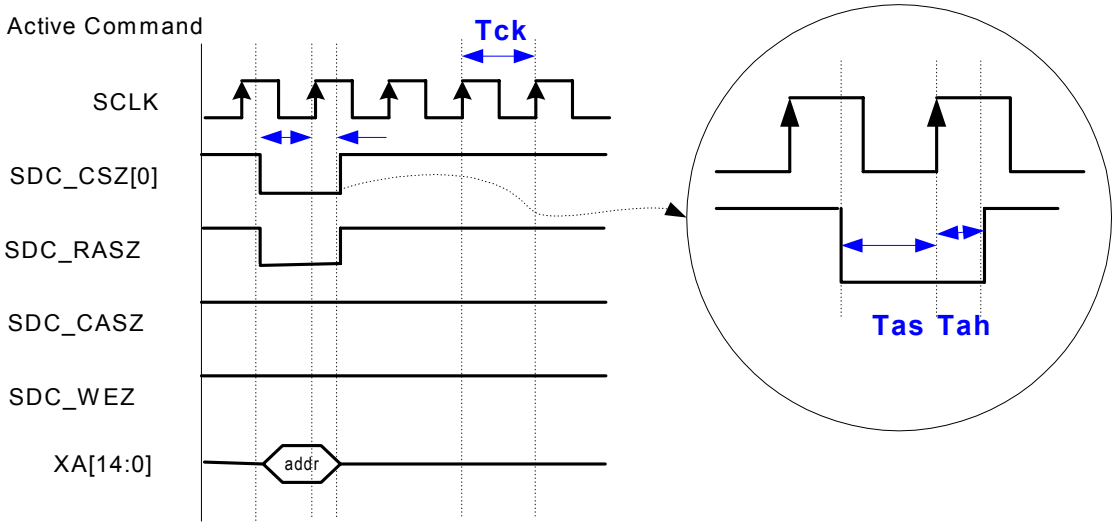


Figure 5-2 Active Command

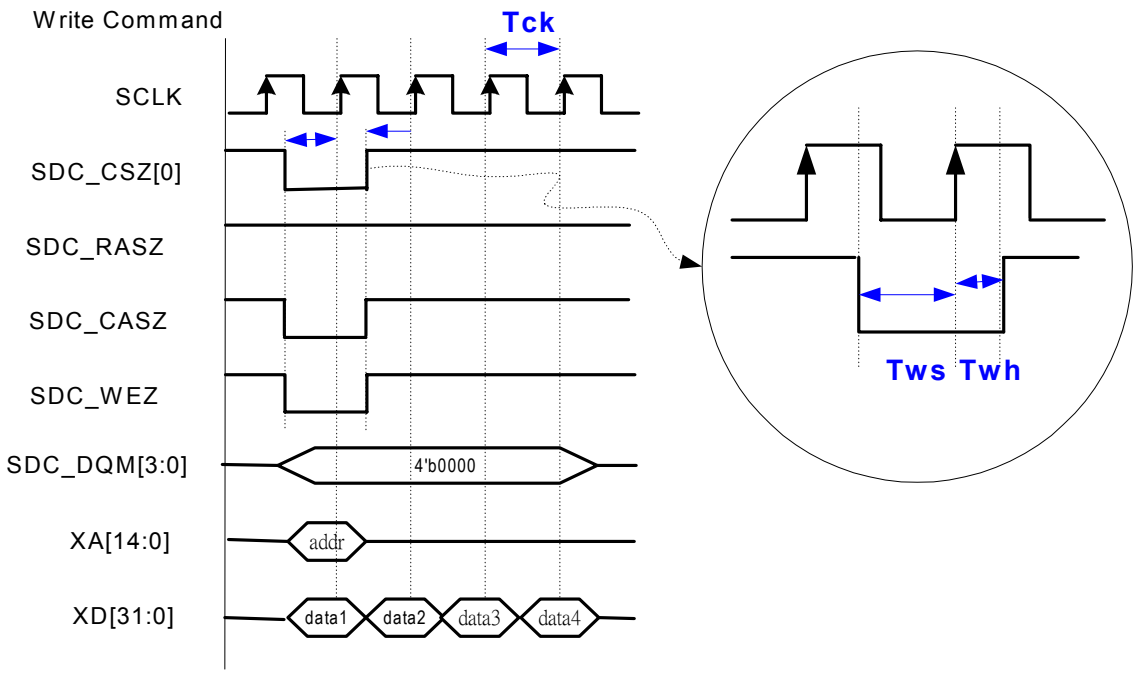


Figure 5-3 Write Command

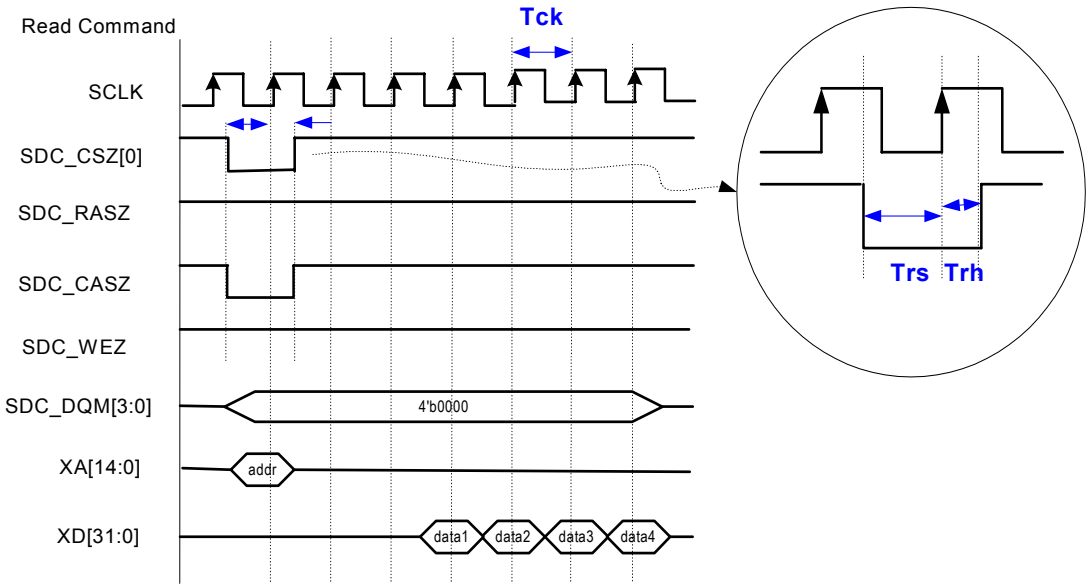
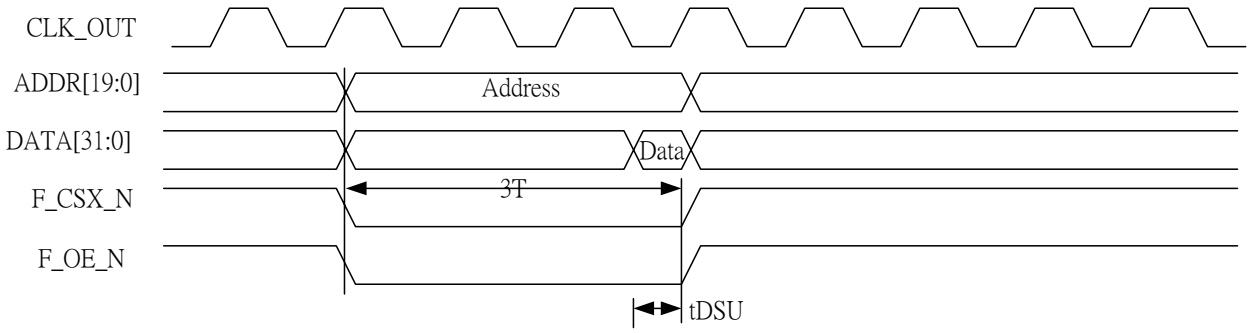


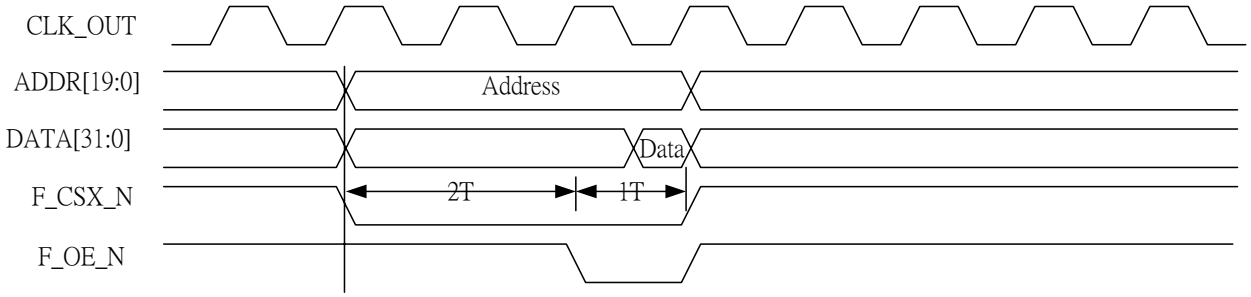
Figure 5-4 Read Command

5.3.2 Memory Bus Read Timing

ROM/FLASH/External Memory: Two wait state Read Timing



ROM/FLASH/External Memory: Two Output enable delay state Read Timing

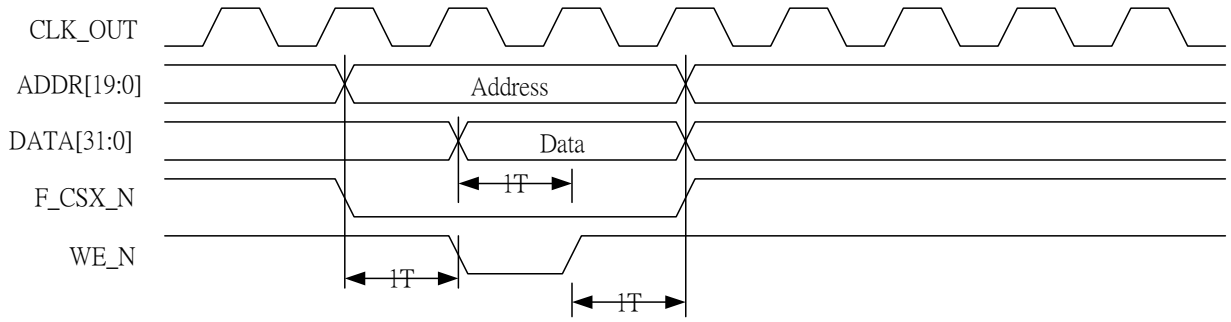


Notes: T is the period of CLK_OUT (11.5ns/87.5Mhz)

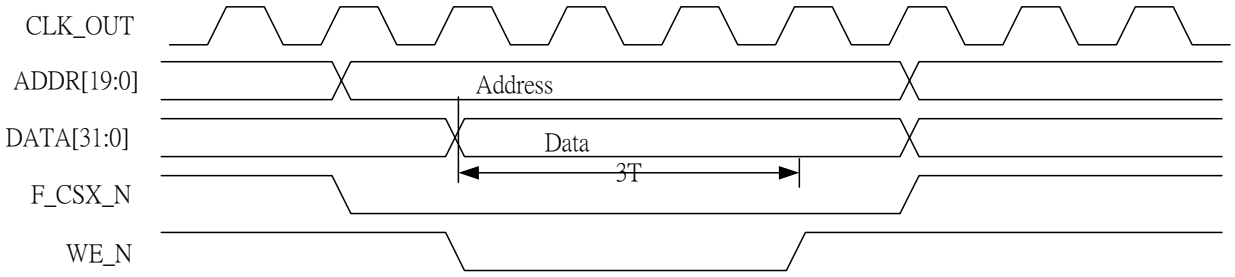
Item	Description	Min	Typ	Max
tRDSU	Data to CLK_OUT rising setup time	TBD	--	--
tRDH	Data to CLK_OUT rising hold time	TBD	--	--
tAC	Address/F_CSX_N pulse width	--	(n+1)T	--
tAOE	Address/F_CSX_N to F_OE_N setup	--	nT	--

5.3.3 Memory Bus Write Timing

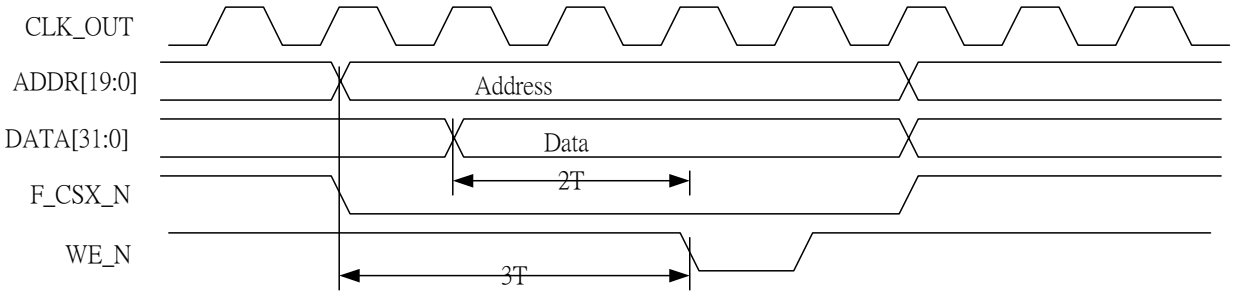
ROM/FLASH/External Memory: Zero Wait state Timing



ROM/FLASH/External Memory: Two Wait state WriteTiming



ROM/FLASH/External Memory: Two Write enable delay state WriteTiming

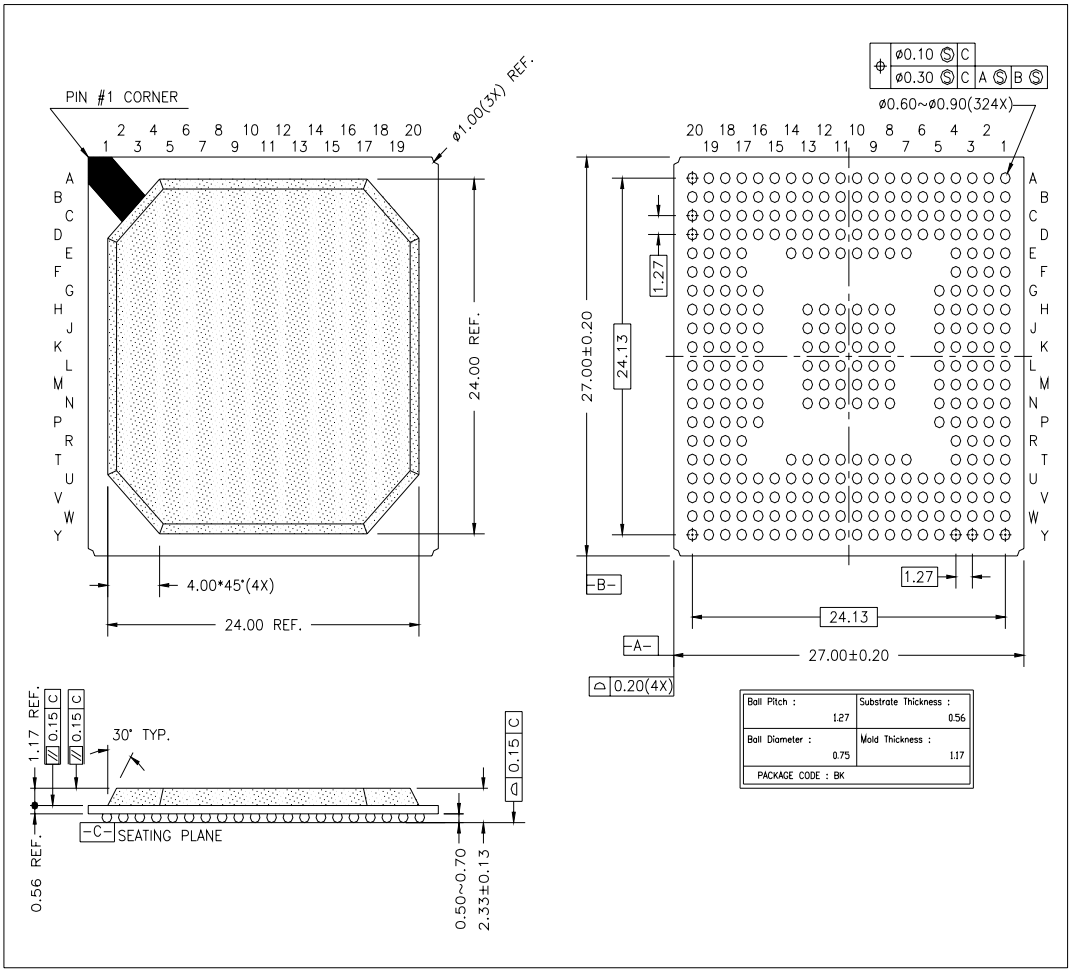


Notes: T is the period of CLK_OUT (11.5ns/87.5Mhz)

Item	Description	Min	Typ	Max
tASU	Adress/CS to WE_N falling setup time	--	(n+1)T	--
tWDSU	Data to WE_N rising setup time	--	(n+1)T	--
tWDH	Data to WE_N rising hold time	--	1T	--
tWEP	WE_N pulse width	--	(n+1)T	--

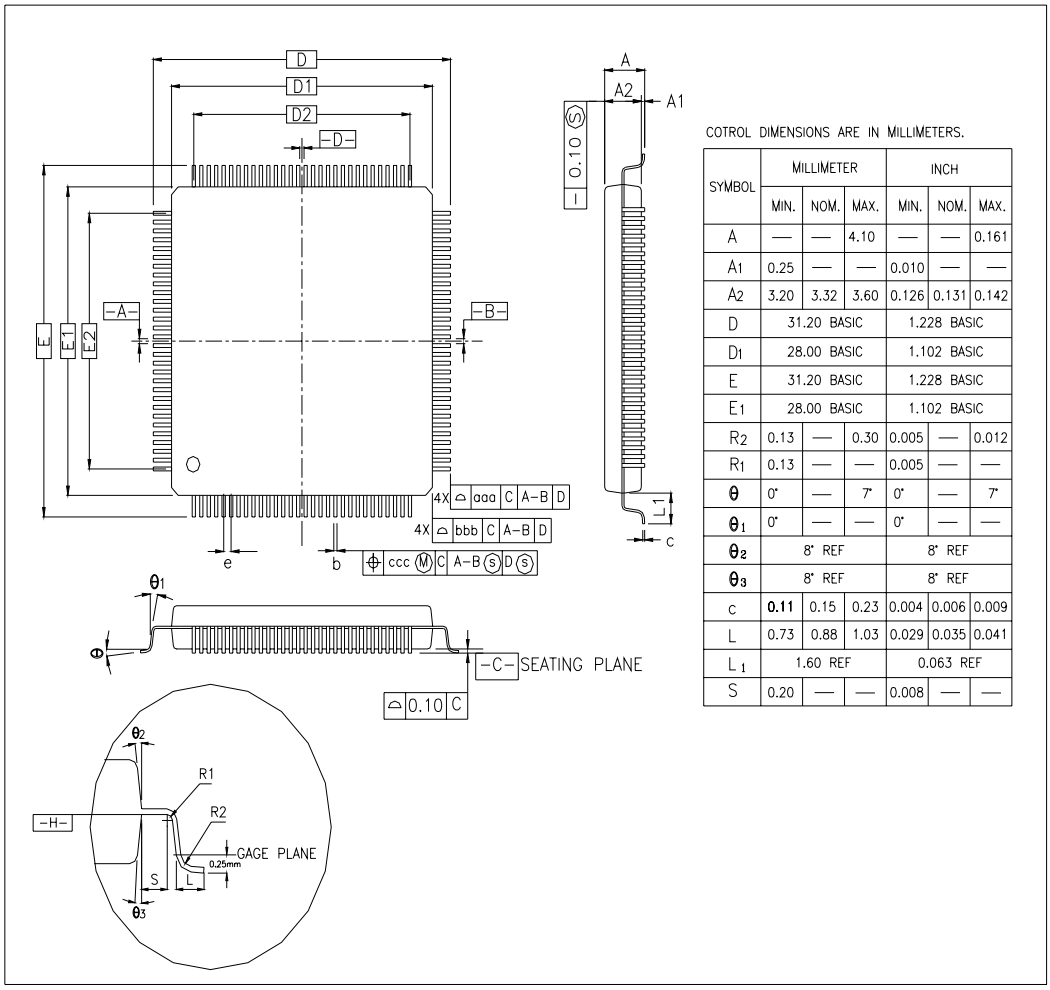
Chapter 6 Packaging

6.1 Ball Grid Array (BGA) 324-pin



Note: Scale = mm

6.2 Plastic Quad Flat Pack (PQFP) 208-pin



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	4.10	—	—	0.161
A_1	0.25	—	—	0.010	—	—
A_2	3.20	3.32	3.60	0.126	0.131	0.142
D	31.20 BASIC			1.228 BASIC		
D_1	28.00 BASIC			1.102 BASIC		
E	31.20 BASIC			1.228 BASIC		
E_1	28.00 BASIC			1.102 BASIC		
R_2	0.13	—	0.30	0.005	—	0.012
R_1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ_1	0°	—	—	0°	—	—
θ_2	8° REF			8° REF		
θ_3	8° REF			8° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L_1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—

Note: Scale = mm

Symbol	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	25.50			1.004		
E2	25.50			1.004		
aaa	0.25			0.010		
bbb	0.20			0.008		
ccc	0.08			0.003		